Bachelor Thesis

Capacitive Arrays for Spatially Resolved Measurements in Nitric Oxide

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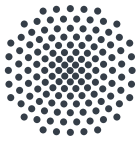

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Stuttgart, 14. August 2024 Hanna Lippmann

Contents

Abstract

Active matrix arrays for spatially resolved measurements were simulated and examined. They were produced on glass substrates using thin film technology. Track and hold circuits with phototransistors were used as array pixels.

Indium-gallium-zinc-oxide thin film transistors with a channel length of 10 µm and channel widths of 10 µm respectively 200 µm were produced and examined. A smaller threshold voltage could be observed for larger channel widths.
The characteristics of the produced phototransistors showed a significant change in the cut-off region for applied light with energetic photons.

Different track and hold circuits were examined, i.e. track and hold circuits consisting of only a transistor and a capacity, track and hold circuits with input buffer, track and hold circuits with output buffer, track and hold circuits with input buffer and output buffer and track and hold circuits with Miller capacity. The achieved results were the best for track and hold circuits with output buffer. Moreover high capacities in the track and hold circuit showed less decrease of the held signal, as the time constant was higher. Therefore the discharging process of the capacity during the holding phase due to the leakage currents of the transistor was slower.
Input currents were used in combination with track and hold circuits and ohmic resistances, switched capacitors or transimpedance amplifiers to convert the currents into voltages.
Track and hold circuits with discharged capacitors were used in combination with input currents and without devices to convert the current into a voltage. After each holding phase, the capacitor was discharged to achieve comparable conditions at the start of each tracking phase. Good results were achieved for high input currents and low frequencies of the track and hold signal.

1:2, 2:4 and 3:8 decoders and multiplexers were simulated and their functionality could be verified. Due to a layout error the realized decoders and multiplexers were not functional and could not be tested.

2x2, 4x4 and 8x8 active matrix arrays were simulated with track and hold circuits with phototransistors and output buffers as array pixels. Their functionality could be verified. Additionally the same arrays controlled by one decoder and one multiplexer were simulated and their functionality could be confirmed as well.
Moreover a 2x2 array was examined physically and its functionality could be shown.

Kurzfassung

Aktiv-Matrix-Anordnungen für räumlich aufgelöste Messungen wurden simuliert und untersucht. Diese wurden auf Glassubstraten mithilfe von Dünnschichttechnologie hergestellt. Als Pixel der Anordnungen wurden Abtast-Halte-Schaltungen mit Phototransistoren und Ausgangsspannungsfolgern verwendet.

Indium-Gallium-Zink-Oxid Dünnschichttransistoren mit Kanallängen von 10 µm und Kanalweiten von 10 µm beziehungsweise 200 µm wurden hergestellt und untersucht. Für große Kanallängen konnten niedrigere Schwellspannungen beobachtet werden.
Die Kennlinien der hergestellten Phototransistoren zeigten signifikante Änderungen im Sperrbereich, wenn Licht mit energetischen Photonen angewandt wurde.

Verschiedene Abtast-Halte-Schaltungen wurden untersucht: Abtast-Halte-Schaltungen, die nur aus einem Transistor und einer Kapazität bestehen, Abtast-Halte-Schaltungen mit Eingangsspannungsfolger, Abtast-Halte-Schaltungen mit Ausgangsspannungsfolger, Abtast-Halte-Schaltungen mit Eingangsspannungsfolger und Ausgangsspannungsfolger, und Abtast-Halte-Schaltungen mit Millerkapazität. Die besten Ergebnisse wurden für Abtast-Halte-Schaltungen mit Ausgangsspannungsfolger erzielt. Außerdem zeigten hohe Kapazitäten in den Abtast-Halte-Schaltungen geringere Abfälle der gehaltenen Signale, weil sie höhere Zeitkonstanten besaßen. Aus diesem Grund war der Entladevorgang der Kapazität während des Haltevorgangs, der aufgrund der Leckströme des Transistors entstand, kürzer.
Eingangsströme wurden in Kombination mit Abtast-Halte-Schaltungen mit Ohm'schen Widerständen, Schaltkapazitäten oder Transimpedanzverstärkern, um die Ströme in Spannungen zu wandeln, verwendet.
Abtast-Halte-Schaltungen mit entladenem Kondensator wurden in Verbindung mit Eingangsströmen verwendet, wenn keine Bauteile zur Strom-Spannungswandlung verwendet wurden. Nach jeder Haltephase wurde der Kondensator entladen, um vergleichbare Bedingungen zu Beginn jeder Abtastphase zu erhalten. Gute Ergebnisse wurden für hohe Eingangsströme und niedrige Frequenzen des Abtast-Halte-Signals erreicht.

1:2, 2:4 und 3:8 Dekoder und Multiplexer wurden simuliert und ihre Funktionalität bestätigt. Aufgrund eines Entwurffehlers waren die realisierten Dekoder und Multiplexer nicht funktionsfähig und konnten nicht getestet werden.

2x2, 4x4 und 8x8 Aktiv-Matrix-Anordnungen wurden simuliert. Abtast-Halte-Schaltungen mit Phototransistoren und Ausgangsspannungsfolger wurden als Pixel der Anordnungen verwendet. Die Funktionalität der Anordnungen konnte bestätigt werden. Zusätzlich wurden die gleichen Anordnungen mit einem Dekoder und einem Multiplexer angesteuert. Dies wurde simuliert und die Funktionalität

konnte ebenfalls bestätigt werden.
Außerdem wurde eine 2x2 Anordnung physisch untersucht und die Funktionalität konnte gezeigt werden.

1 Introduction

This work is part of the quantum nitric oxide sensing experiment (QNOSE) at the 5th institute of physics at the university of Stuttgart. The aim of the QNOSE project is the processing of a sensor to detect nitric oxide (NO). Therefore NO is excited into rydberg states by lasers. In the relaxation process ultraviolet fluorescence light is emitted, which can be detected [14].
Moreover an array of electrodes can be used as measurement array and a screenshot of the spatially resolved NO signal can be taken.

To detect ultraviolet light, indium-gallium-zinc-oxide (IGZO) phototransistors are used, as the bandwidth of IGZO is over 3.0 eV [5]. The drain current of the phototransistor is proportional to the incident ultraviolet light and can be measured using track and hold circuits. Like this it is possible to track the light intensity in form of a voltage, hold this signal and read it out at a later time.

In this work different track and hold circuits and possibilities to convert currents into voltages are examined. The circuits are produced on glass substrates using thin film technology. Like this it is possible to integrate the circuits into the cell of the QNOSE project.
Moreover the track and hold circuits are used as pixels in active matrix arrays. The individual pixels are all in the tracking phase at the same time and a picture of this situation is present in the holding phase. In this phase the pixels can be read out and spatially resolved measurements in form of screenshots are possible. Decoders and multiplexers are designed using thin film technology and they are produced on the same glass substrate as the arrays. Like this it is possible to control the arrays and reduce the signal path between control and array. This leads to less noise influencing the measured signal.

First the theoretical background of the developed circuits is discussed in section 2. Therefore transistors, operational amplifiers, capacities, different track and hold circuits and logical circuits are explained.
The created capacities and resistances using thin film technology, as well as the fabrication of the thin film structures, are presented in section 3.
In section 4 the different circuits are discussed and compared concerning the simulated and measured results.

2 Theoretical Background

In the following the theoretical background to understand the design and working principle of capacitive arrays for spatially resolved measurements is explained.

2.1 Transistors

Transistors are very important when realizing circuits like capacitive arrays for spatially resolved measurements as they work as switches. They are for example needed in track and hold circuits like explained in section 2.5 or in logical circuits like explained in section 2.6.
Thin film transistors (TFTs) are made up of three electrodes, the drain, the gate and the source. Depending on the potential applied at the gate, drain and source are either connected or not. The characteristic between drain current I_D and drain source voltage V_{DS} can be seen in fig. 1 for different gate source voltages V_{GS} [6].

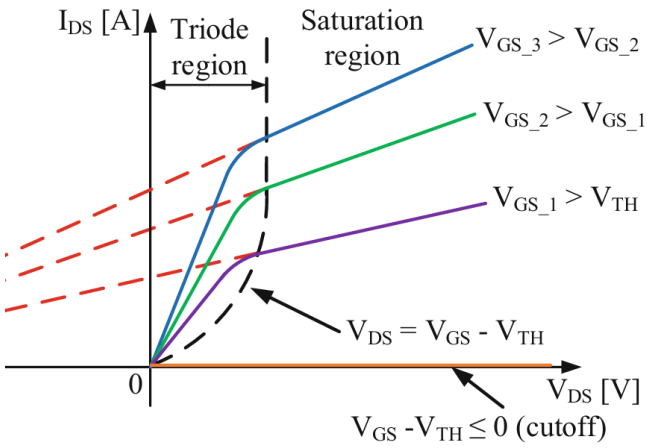


Fig. 1: The characteristic between drain current I_D and drain source voltage V_{DS} is shown for different gate source voltages V_{GS}. The different regions are explained in section 2.1.2. The graphic is taken from [17].

2.1.1 Thin Film Transistors

Thin film transistors (TFTs) are realized by depositing different layers on a glass substrate. A possible layer structure of TFTs, as used during this work, is shown in fig. 2. The bottom gate layer is deposited on the glass substrate and on top of the gate material one dielectric layer is deposited. Afterwards the drain and source layer is deposited on the substrate and the drain and the source contacts of the transistor are created using photolithographic structuring as described in section 3.1.1. On top of the drain and source layer, one semiconductor layer is deposited and then again a dielectric layer follows. Lastly the top gate is created by depositing a conductive layer as gate material [3].

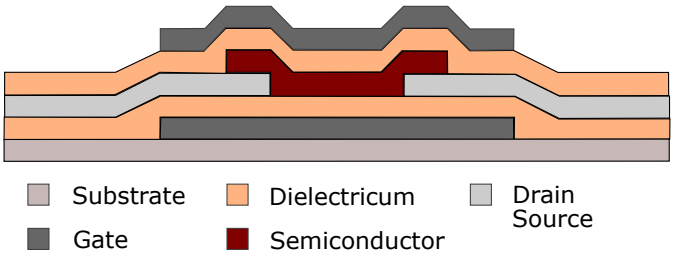


Fig. 2: The layer structure of a dual gate thin film transistor is shown. It consists of different layers: substrate, gates, dielectricum, semiconductor and drain and source.

2.1.2 Analytical Description

The voltage and current properties of TFTs, as used during this work, can be described by the equations of n-channel MOSFETs. As seen in fig. 1 there are different regions concerning the characteristics between drain current and gate source voltage.

Cut-off Region
In the cut-off region the gate source voltage V_{GS} is below the cut-in voltage V_{on}. Therefore in theory no drain current I_{D} is present,

$$I_{\mathrm{D}} = 0 \qquad \text{for} \quad V_{\mathrm{GS}} < V_{\mathrm{on}} \tag{2.1}$$

holds. In reality there are small currents present due to leakage currents through the semiconductor or the gate dielectricum [10].

Subthreshold Region
If the gate source voltage V_{GS} is increased above the cut-in voltage V_{on} but still below the threshold voltage V_{th}, the TFT works in the so called subthreshold region. In this region an exponential dependency between the drain current I_{D} and the gate source voltage exists. It holds

$$I_{\mathrm{D}} \propto \exp\left(\frac{V_{\mathrm{GS}}}{T}\right) \qquad \text{for} \quad V_{\mathrm{on}} < V_{\mathrm{GS}} < V_{\mathrm{th}} \tag{2.2}$$

where T is the temperature. The exponential dependency can be explained by the thermal energy of the charge carriers. If the thermal energy is high enough i.e. if the temperature is high enough, the charge carriers can get into the semiconductor by transcending the energy barrier at the source contact and diffuse to the drain contact [10].

Triode Region
By increasing the gate source voltage V_{GS} even further, the triode or linear region of the TFT is reached. In this case the drain source voltage V_{DS} has to be smaller than the difference between the gate source voltage and the threshold voltage V_{th}.

As the name suggests, a linear dependency between drain current and gate source voltage exists. It holds

$$I_{\mathrm{D}} = \frac{\mu \cdot C_{\mathrm{diel}} \cdot w}{l} \left((V_{\mathrm{GS}} - V_{\mathrm{th}}) \cdot V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right) \qquad \text{for} \quad 0 < |V_{\mathrm{DS}}| < |V_{\mathrm{GS}} - V_{\mathrm{th}}| \tag{2.3}$$

where μ denotes the mobility of the charge carriers, C_{diel} the capacity per unity area of the dielectricum, w the channel width of the transistor and l the channel length of the transistor. For small drain source voltages the term $-\frac{V_{\mathrm{DS}}^2}{2}$ in eq. (2.3) can be neglected and it is possible to define a resistance R between drain and source. By comparing eq. (2.3) with Ohm's law

$$R = \frac{l}{\mu \cdot C_{\mathrm{diel}} \cdot w \cdot (V_{\mathrm{GS}} - V_{\mathrm{th}})} \tag{2.4}$$

results. Therefore this region is also called resistance region [10].

Saturation Region
For drain source voltages V_{DS} higher than the difference between gate source voltage V_{GS} and threshold voltage V_{th}, the TFT works in the saturation region. In this case the drain current I_{D} is independent of the drain source voltage for ideal transistors. As seen in fig. 1, the drain current rises for increasing drain source voltages. This is due to channel length modulation. Moreover the drain current has a quadratic dependency of the gate source voltage. It holds [10]

$$I_{\mathrm{D}} = \frac{\mu \cdot C_{\mathrm{diel}} \cdot w}{l} \cdot (V_{\mathrm{GS}} - V_{\mathrm{th}})^2 \tag{2.5}$$

$$I_{\mathrm{D}}(V_{\mathrm{DS}}) = \text{const} \qquad \text{for} \quad 0 < |V_{\mathrm{GS}} - V_{\mathrm{th}}| < |V_{\mathrm{DS}}| \tag{2.6}$$

2.1.3 Phototransistor

Phototransistors are one option to realize sensors to detect light with sufficient energy using thin film technology. The energy of the photons needs to be higher than the energy gap between valence band and conducting band. The structure of thin film phototransistors is similar to the structure of TFTs presented in section 2.1.1 with the difference that phototransistors are build without top gate.
If no light is applied to the phototransistor, the characteristic between drain current and gate source voltage is similar to the one of normal TFTs. By applying light with sufficient energy to the phototransistor, the characteristic between drain current and gate source voltage changes significantly for negative gate source voltages. Electron-hole pairs are created leading to a higher concentration of charge carriers and therefore to a smaller threshold voltage. This leads to an increased drain current for negative gate source voltages in comparison to the characteristics without applied light with sufficient energy. By measuring the drain current, it is possible to determine the applied light power [4].

2.2 Indium-Gallium-Zinc-Oxide

Indium-Gallium-Zinc-Oxide (IGZO) is a semiconductor used in displays or sensor applications. The conducting band of IGZO is formed of spatial s orbitals. As s orbitals are of spherical symmetry the overlap is approximately the same for crystalline and amorphous structure and therefore the mobility of the charge carriers stays also the same. Furthermore IGZO has high electrical performance, large-area uniformity and can be processed at low temperature. Therefore it is often used as semiconductor in TFTs. With a wide bandgap over 3.0 eV, IGZO is transparent in the visible and has a high response to light in the ultraviolet. Thus IGZO TFTs can be used as phototransistors for the detection of ultraviolet light [5].

2.3 Operational Amplifiers

Operational amplifiers are important devices when investigating voltage signals. In fig. 3 the schematic structure of an operational amplifier (opamp) is shown. Opamps have pins for the supply voltage, one for the positive (V_{DD}) and one for the negative (V_{SS}) supply voltage, pins for the input and one pin for the output (V_{out}). There are two input pins, one for the inverting input (V_-) and one for the non-inverting input (V_+).

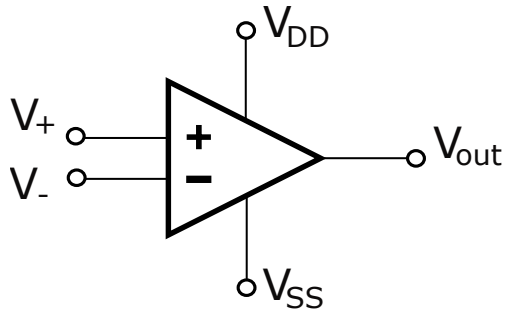


Fig. 3: The circuit symbol of an operational amplifier consisting of pins for positive (V_{DD}) and negative (V_{SS}) supply voltage, inverting (V_-) and non-inverting (V_+) input and output (V_{out}) is shown.

For an ideal opamp, the input resistances are infinitely high leading to zero input currents. In comparison the output resistance is zero and therefore the opamp output works as an ideal voltage source. Opamps amplify the voltage difference between the inverting and the non-inverting input leading to an output voltage of

$$V_{\mathrm{out}} = A_0 \cdot (V_+ - V_-)\,, \tag{2.7}$$

where A_0 denotes the open loop amplification and V_- and V_+ are the voltages at the inverting and non-inverting inputs. For an ideal opamp $A_0 = \infty$ holds. However the output voltage of the opamp has its maximum at the positive supply voltage and its minimum at the negative supply voltage [13].

2.3.1 Open Loop Configuration

The easiest opamp circuit is created when setting the inverting or the non-inverting input to ground. Like that the output voltage can be described as

$$V_{\text{out}} = A_0 \cdot V_+ \qquad \text{for} \quad V_- = 0 \tag{2.8}$$

$$V_{\text{out}} = -A_0 \cdot V_- \qquad \text{for} \quad V_+ = 0. \tag{2.9}$$

eq. (2.8) holds when the inverting input is set to ground and eq. (2.9) holds when the non-inverting input is set to ground [13].

2.3.2 Unity Gain Amplifier

An important usage of opamps are buffers. In this case the output of the opamp is fed back to the inverting input as shown in fig. 4. Like that the voltages at the output and inverting input are identical. As the opamp tries to set the potential difference between the inputs to zero, after a short time both inputs and the output have the same voltage. Therefore the gain is one and the opamp circuit is called unity gain amplifier or voltage follower.

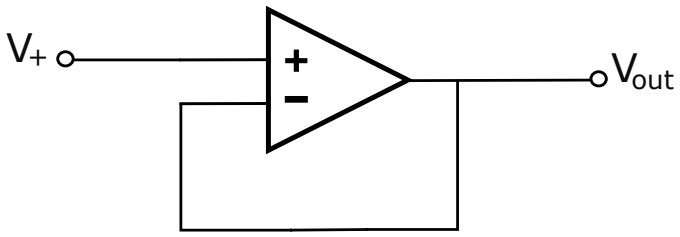


Fig. 4: A circuit for an operational amplifier working as a unity gain amplifier is shown. The inverting input is connected to the output of the operational amplifier.

The advantage of unity gain amplifiers is, that the signals at the input and the output are decoupled. Therefore buffers are mainly used in circuits with different impedances to prevent charging or discharging of one resistance by the others [8]. Unity gain amplifiers are used in track and hold circuits as explained in section 2.5.

2.3.3 Transimpedance Amplifier

It is possible to convert currents to voltages by using opamps. In this case the non-inverting input is set to ground and the inverting input is connected to the output by a resistance R_{f} as shown in fig. 5. By applying a current I_{in} at the input

$$V_{\text{out}} = -R_{\text{f}} \cdot I_{\text{in}} \tag{2.10}$$

holds for the output voltage V_{out}. The amplification

$$A = \frac{V_{\text{out}}}{I_{\text{in}}} = -R_{\text{f}} \tag{2.11}$$

is also called transimpedance leading to the name transimpedance amplifier for this opamp circuit [15].

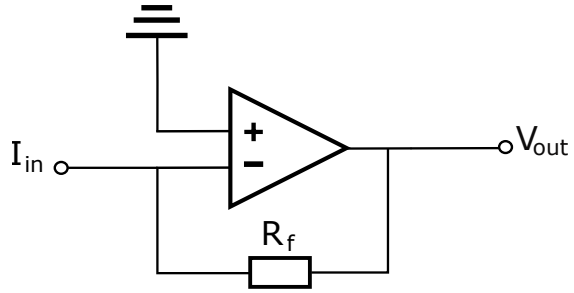


Fig. 5: A circuit for an operational amplifier working as a transimpedance amplifier is shown. The non-inverting input is set to ground, whereas the inverting input is connected to the output by a resistance R_f.

2.4 Capacities

Capacities are able to store charges and can therefore be used in track and hold circuits as explained in section 2.5. The behaviour while charging and discharging the capacity is important, as it influences the tracking and holding phase of the track and hold circuit. The charging and discharging process is shown in fig. 6 in black for the charging process and in grey for the discharging process.

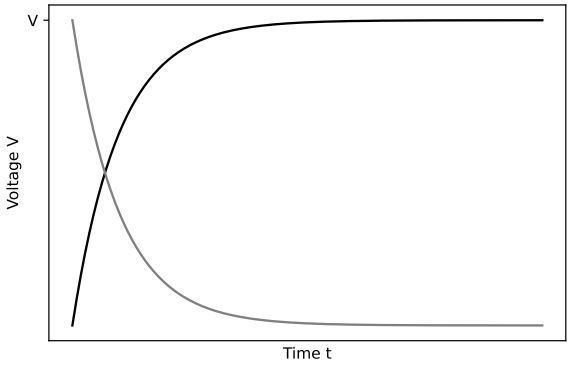


Fig. 6: In black the charging process of a capacity and in grey its discharging process is shown.

If a capacity is charged and discharged, it holds

$$V_{\mathrm{C_{charge}}}(t) = V \cdot \left(1 - \exp\left(-\frac{t}{R_\mathrm{C} \cdot C}\right)\right) \tag{2.12}$$

$$V_{\mathrm{C_{discharge}}}(t) = V \cdot \exp\left(-\frac{t}{R_\mathrm{C} \cdot C}\right) \tag{2.13}$$

for the voltage V_C at the capacity. Here V denotes the input voltage at the capacity, t the time after the charging or discharging process has started, R_C the resistance of the capacity and C the capacity [13].

2.5 Track and Hold Circuits

Track and hold circuits can be used to track an input signal during the tracking phase and holding it during the hold phase. Like that a signal can be detected and read out at a later time. There are different ways to realize track and hold circuits.

2.5.1 Track and Hold Circuit consisting of a Transistor and a Capacity

The easiest track and hold circuit consists of a transistor and a capacity. It is shown in fig. 7. The transistor works as a switch depending on the gate voltage (CLK signal) as described in section 2.1.1. The capacity is charged by the voltage that wants to be detected. After the capacity is separated from the input signal by the transistor, the capacity stays charged and the voltage can be read out [12].

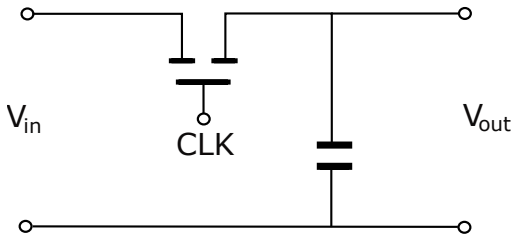


Fig. 7: A track and hold circuit consisting of a transistor working as a switch and a capacity is shown.

2.5.2 Track and Hold Circuit with Input Buffer

A more complex version of a track and hold circuit is created by adding an input buffer like shown in fig. 8. In this case the input signal and the signal being tracked and held are decoupled. This improves the held signal as it is independent of the changing input signal. In addition the input buffer has a low impedance output and therefore the capacity is able to charge quickly. Like this higher frequencies of the track and hold clock are possible [16].

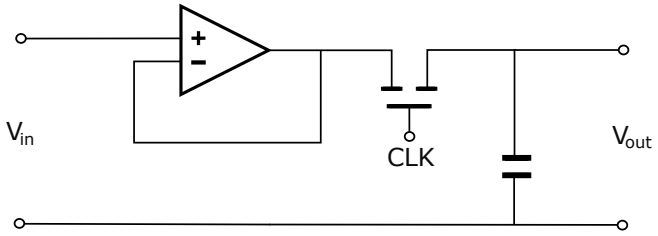


Fig. 8: A track and hold circuit with input buffer is shown.

2.5.3 Track and Hold Circuit with Output Buffer

The easiest way to detect the tracked and held output signal is by connecting it to an oscilloscope. As oscilloscopes have input resistances of 1 MΩ, it is necessary to add an output buffer between the capacity and the oscilloscope as shown in fig. 9. The output buffer has a high input impedance so that the capacity is not discharged by the oscilloscope [16].

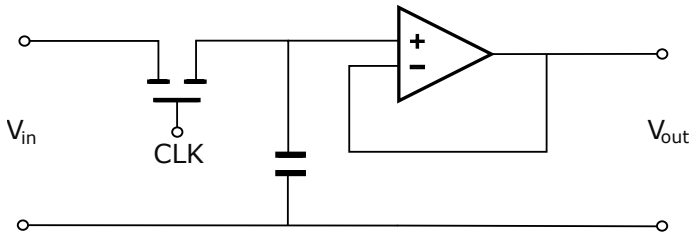


Fig. 9: A track and hold circuit with output buffer is shown.

2.5.4 Track and Hold Circuit with Input Buffer and Output Buffer

It is also possible to realize track and hold circuits with input and output buffers as shown in fig. 10. As a combination of section 2.5.2 and section 2.5.3 this version of track and hold circuits has the advantage that the capacity is charged quickly and is not discharged by the oscilloscope.

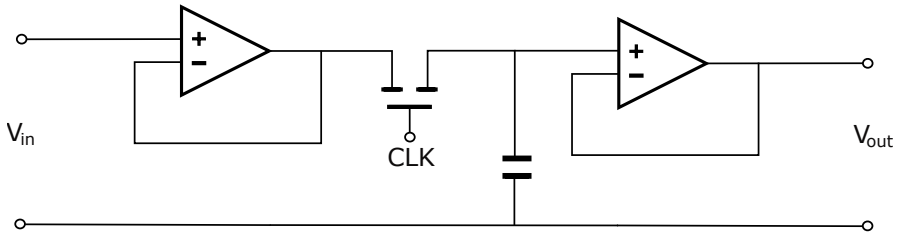


Fig. 10: A track and hold circuit with input and output buffer is shown.

2.5.5 Track and Hold Circuit with Miller Capacity

A track and hold circuit with Miller capacity can be used to improve the hold phase. As shown in fig. 11 this circuits consists of two capacities, two transistors as switches, one operational amplifier and one output buffer.

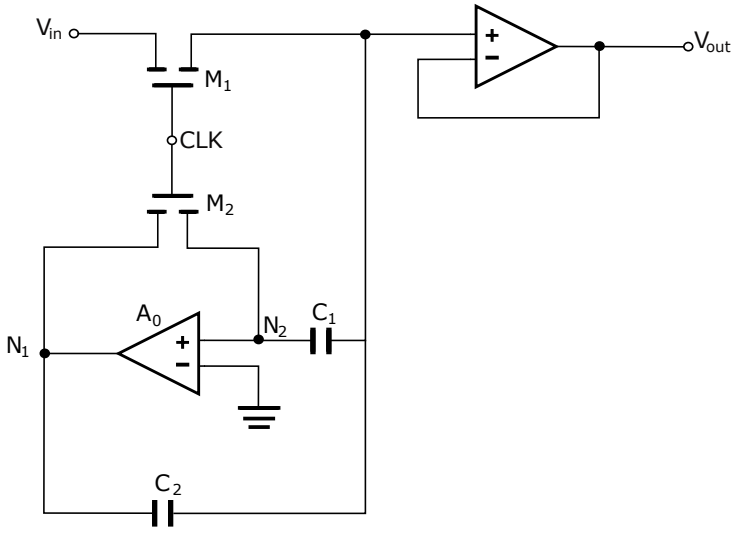


Fig. 11: A track and hold circuit with miller capacity is shown. It consists of two transistors M_1 and M_2 working as switches, two capacities C_1 and C_2 and one operational amplifier with amplification A_0. In addition there is an output buffer used.

In the tracking phase the two switches M_1 and M_2 are closed and the capacities C_1 and C_2 are tracking the signal. Due to the operational amplifier A_0, the nodes N_1 and N_2 are on virtual ground. In the holding phase the switches M_1 and M_2 are open leading to an effective hold capacity of

$$C_{\text{hold}} = \frac{A_0 \cdot C_2}{C_1 + C_2}. \tag{2.14}$$

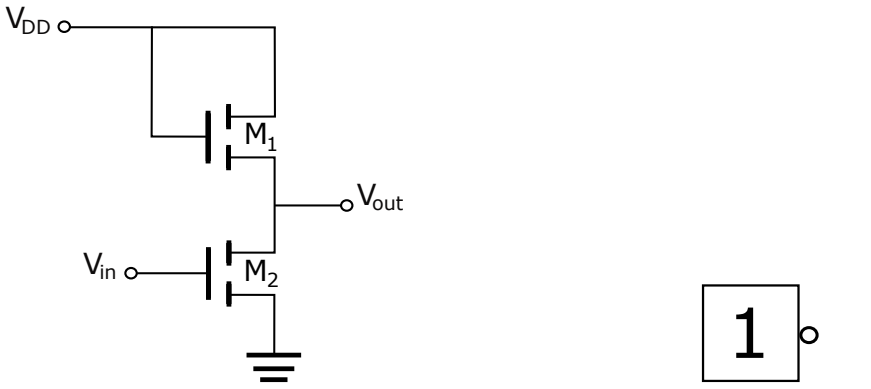
In comparison to the capacity in the tracking phase, the one in the holding phase is bigger leading to a more stable hold signal. As seen in eq. (2.14) the capacity is proportional to the gain of the operational amplifier so that a higher gain leads to better holding signals [7].
With the Miller capacity it is possible to achieve different capacities in the tracking and holding phase. The capacity in the tracking phase is low so that the capacity is charged quickly as seen in eq. (2.12). In comparison the capacity in the holding phase is higher to reach a more stable holding signal as seen in eq. (2.13).

2.6 Logical Circuits

Logical circuits are used to generate one or more output signals in dependence of the input signals. Like this decoders or multiplexers can easily be realized by transistors. In the following the design of decoders and multiplexers as well as the needed NOT, NAND and AND circuits are described using positive logic. In this case high voltages are related to the Boolean variable 1 and low voltages to the Boolean variable 0 [11].

2.6.1 NOT

The NOT circuit is the easiest logical circuit. As the name suggests the aim of a NOT circuit is the inversion of a given input signal. As shown in fig. 12 the circuit consists of two transistors. If the input signal is high, the transistor M_2 is conductive and the output signal is connected to ground leading to a low output signal.
In the following the transistor is called closed if the transistor is conductive and the switch is therefore closed and it is called open if the switch is open and the transistor is not conductive.
If the input signal is low, the transistor M_2 is open and the output signal is not connected to ground. As the transistor M_1 is connected to positive supply voltage it is always closed and like that the output signal is also high. The truth table as shown in table 1 results [11].



(a) Realisation by two transistors in series (b) Circuit symbol

Fig. 12: The realisation and the circuit symbol of a NOT circuit are shown.

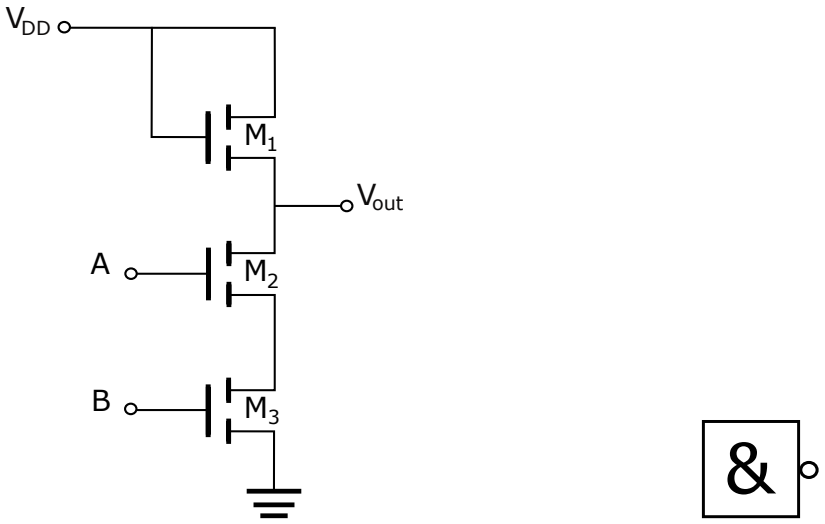
Tab. 1: The truth table of the NOT circuit is shown. In denotes the input signal and Out the output signal.

In	Out
1	0
0	1

2.6.2 NAND

The aim of a NAND circuit is to create an output signal being only high if the two input signals are low. As two input signals are needed the design is a bit more complex as for the NOT circuit. As seen in fig. 13 three transistors are connected in series. The working principle is similar to section 2.6.1. If both transistors, connected to the input signals A and B, are closed, the output signal is connected to ground. If at least one input signal is low, meaning at least one of the transistors

M_2 or M_3 is open, the output signal is connected to positive supply voltage through the transistor M_1. The truth table can be seen in table 2 [11].



(a) Realisation by three transistors in series (b) Circuit symbol

Fig. 13: The realisation and the circuit symbol of a NAND circuit are shown.

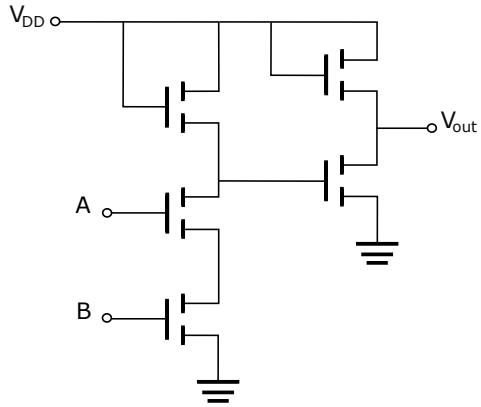
Tab. 2: The truth table of the NAND circuit is shown. A and B denote the input signals and Out denotes the output signal.

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

A NAND circuit for n input signals can be realized by connecting $n+1$ transistors in series. The first transistor M_1 is connected to positive supply voltage whereas the other transistors are connected to the input signals and to ground as shown in fig. 13.

2.6.3 AND

The aim of AND circuits is to create a high output signal only if both input signals are high. It can be realized by a parallel connection of a NOT and a NAND circuit as shown in fig. 14. Like this the output signal created from the NAND circuit is inverted by the NOT circuit and the truth table in table 3 results [11].



(a) Realisation by parallel connection of NAND and NOT

(b) Circuit symbol

Fig. 14: The realisation and the circuit symbol of an AND circuit are shown.

Tab. 3: The truth table of the AND circuit is shown. A and B denote the input signals and Out denotes the output signal.

A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

AND circuits for n inputs signals can be created by using a NAND circuit for n inputs instead of the NAND circuit with two inputs.

2.6.4 Decoder

NOT and AND circuits can be used to create decoders which are used to convert a n-bit number generated by n input signals, being either high or low, to a m-bit number represented by m output signals, being as well either high or low. Like this it is possible to transfer each combination of input signals to one output. The output with the highest number denotes the most significant bit and the output with the lowest number denotes the least significant bit [2].

Decoder 1:2
The easiest decoder is a decoder transferring one input signal A to two independent output signals 1 and 2. To realize a 1:2 decoder an enable signal E is necessary in addition to the given input signal as seen in fig. 15. The enable signal is always high and is necessary to realize the two AND circuits so that it is possible to have two output signals. The truth table is shown in table 4.

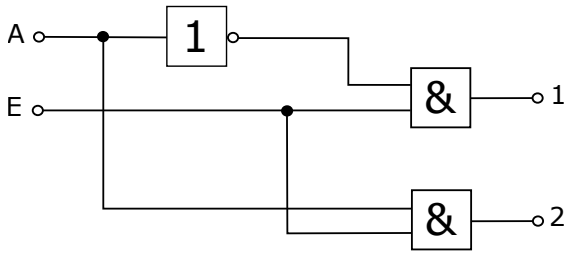


Fig. 15: A 1:2 decoder realized with NOT and AND circuits is shown. A denotes the input signal whereas E denotes the needed enable signal. 1 and 2 are the two outputs of the decoder.

Tab. 4: The truth table of a 1:2 decoder is shown. A is the input signal, E the enable signal and 1 and 2 are the two output signals.

A	E	2	1
0	1	0	1
1	1	1	0

Decoder 2:4

A decoder transferring two input signals A and B into four output signals 1-4 is called a 2:4 decoder. In this case no enable signal is necessary because the inputs of the AND circuits are given by the possible combinations of the input signals A and B and the inverted ones. The schematic design is shown in fig. 16. The truth table is shown in table 5.

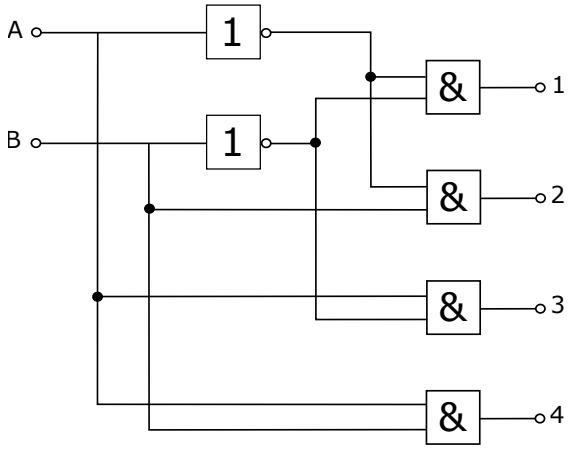


Fig. 16: A 2:4 decoder realized with NOT and AND circuits is shown. A and B denote the input signals and 1-4 are the four outputs of the decoder.

Tab. 5: The truth table of a 2:4 decoder is shown. A and B are the input signals and 1-4 are the four output signals.

A	B	4	3	2	1
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Decoder 3:8

A 3:8 decoder is similar to the 2:4 decoder with the difference that there are three input signals A-C and eight output signals 1-8. Moreover AND circuits with three inputs are necessary. The schematic design is shown in fig. 17. The truth table is shown in table 6.

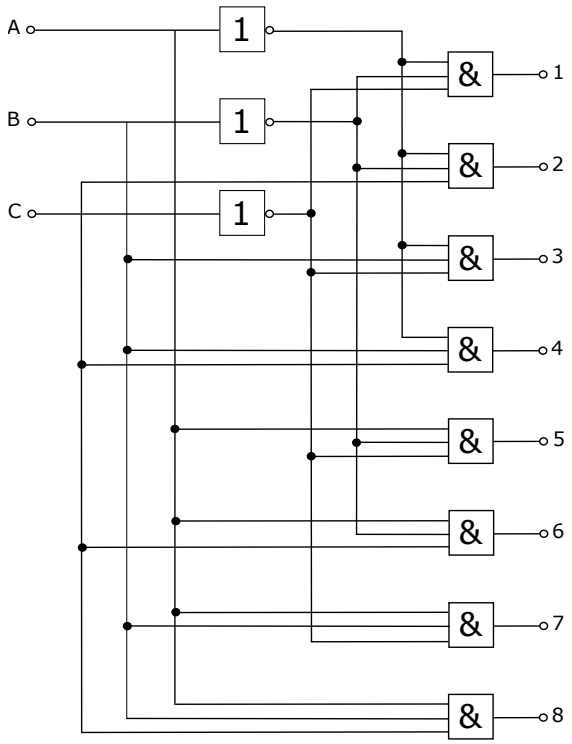


Fig. 17: A 3:8 decoder realized with NOT and AND circuits is shown. A-C denote the input signals and 1-8 are the eight outputs of the decoder.

Tab. 6: The truth table of a 3:8 decoder is shown. A-C are the input signals and 1-8 are the eight output signals.

A	B	C	8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

2.6.5 Multiplexer

Multiplexers are devices similar to decoders and have only one output to detect the different possible output signals. This is realized by adding transistors working as switches at the outputs of the decoder as shown in fig. 18 for the 2:1 multiplexer. Other multiplexers can be realized analogously.
The drains of the transistors are connected to the corresponding signal that wants to be detected for the given input signals. The sources of the transistors are connected to the output signal of the multiplexer and the gates are connected to the outputs of the decoder. Like this the output signal of the multiplexer corresponds to the high output of the decoder. As seen in section 2.6.4 only one output of the decoder is high for given input signals. Therefore only one switch is closed and the output of the multiplexer only consists the right signal. If the multiplexer wants to be used without external input signals (Input 1 and 2) the drains of the transistors can be connected to the corresponding outputs of the decoder. Like this the outputs of the decoder depending on the inputs of the decoder can be measured at the output of the multiplexer [2].

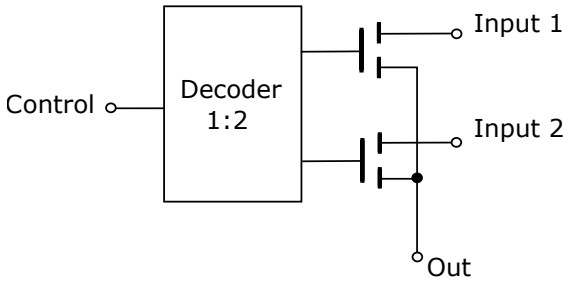


Fig. 18: A 2:1 multiplexer is realized by adding transistors as switches to the outputs of the decoder. By connecting the drains of the transistors to external signals (Input 1 and Input 2) it is possible to switch between these signals by applying the correct control signals at the decoder.

3 Fabrication

In the following the fabrication of thin film structures like TFTs, resistances and capacitors is explained.

3.1 Thin Film Technology

To produce thin film items as transistors, resistances or capacities, different layers are deposited on a glass substrate. This is shown in fig. 2 for the TFT. Therefore a layout has to be developed for the designed circuits and lithography masks are produced for each layer.

3.1.1 Photolithographic Structuring

The general production steps are the same for each layer. After the layer is deposited on the whole substrate, photolithographic structuring is used. This process is schematically shown in fig. 19 for positive photoresist. First the photoresist is deposited on the glass substrate using spin coating. Then the photoresist is exposed using the mask of the layer. Afterwards the resist is developed and the exposed photoresist is removed. Like that the photoresist only is present at places where the deposited layer is meant to be. To remove the layer from the undesired places on the substrate, the next step in the production is etching. During the production wet chemical etching and reactive ion etching are performed. After this step, the remaining photoresist is stripped and the substrate with desired layer structure remains.

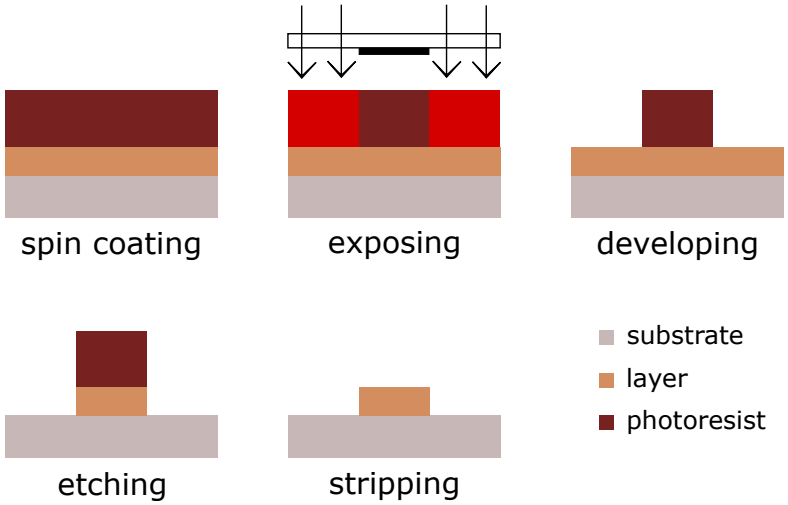


Fig. 19: The process of photolithographic structuring containing the steps spin coating, exposing, developing, etching and stripping is shown.

3.1.2 Deposition of the Layers

Firstly the bottom gate layer is created. Therefore one layer of 70 nm Molybdenum Tantalum (MoTa) is deposited using magnetron sputtering.
Afterwards a double layer of 175 nm silicium nitrite (SiN) and 50 nm silicium oxide (SiOx) is deposited using plasma enhanced chemical vapour deposition (PEVCD). This layer creates the dielectricum between bottom gate and drain/source.
The drain/source layer is a double layer containing 70 nm of MoTa and 50 nm of indium tin oxide (ITO). First the MoTa layer is produced using the negative NOMOTA mask in the photolithographic structuring. Like that MoTa is removed at the places, where the semiconductor is going to be. This is necessary as MoTa extracts oxygen from the semiconductor, leading to negative influence on the transistor characteristics [15]. ITO does not show this influence and is therefore deposited between the MoTa and the IGZO layer.
The semiconductor layer is realized by depositing 35 nm of IGZO using magnetron sputtering. The following dielectric layer consits of 130 nm SiOx which is deposited using PECVD.
Lastly the top gate is realized by depositing 70 nm MoTa and 50 nm ITO. As this double layer is not in direct contact with the semiconductor, MoTa has not to be removed and there is no need to use the NOMOTA mask during the photolithographic structuring [3].

3.2 Resistances

There are two ways of creating resistances for thin film applications. On the one hand ohmic resistances with fixed values can be created and on the other hand resistances, which are adjustable after the fabrication, can be realized by switched capacitors.

3.2.1 Ohmic Resistance

Realisation
Ohmic resistors are easy to use in electrical circuits as they only need to be connected with two wires. For thin film applications they can be realized by the ITO layer. This is achieved by depositing the drain/source layer and removing the MoTa by using the negative NOMOTA mask. As explained in section 3.1 the drain/source layer is a double layer containing MOTA and ITO. In the overlapped areas of the drain/source and the NOMOTA mask, a layer containing only ITO results.
The resistance of a ITO wire is given by

$$R = R_{\square} \cdot \frac{l}{w} \quad , \tag{3.1}$$

where $R_{\square} = 47.32\,\Omega/\square$ denotes the sheet resistance, $\square = 1 \cdot 10^{-10}\,\mathrm{m}^2$ is the unit area, l the length and w the width of the ITO wire.

To achieve high resistances it is necessary to create large lengths and small widths of the ITO layer. Therefore it is reasonable to produce the ITO layer in meanders as shown in fig. 20. The meander structure makes the calculation of the resistance more complicated as the squares in the corners have different sheet resistances. Whereas the normal pieces have sheet resistances of $1 \cdot R_\square$, the corner pieces have only sheet resistances of $0.55 \cdot R_\square$ [15].

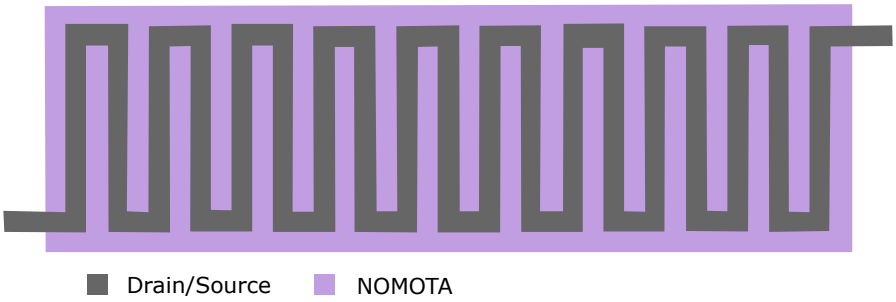


Fig. 20: The ohmic resistance is realized by a meander shaped ITO path. The needed Drain/Source and NOMOTA masks are shown.

To simplify the calculation, unit cells as shown in fig. 21 are used. Like that the resistance can be calculated by

$$\begin{aligned} R &= 2 \cdot R_\square \cdot \frac{l}{10\,\mu\text{m}} + 2 \cdot R_\square \cdot \frac{10\,\mu\text{m}}{10\,\mu\text{m}} + 4 \cdot R_\square \cdot \frac{10\,\mu\text{m}}{10\,\mu\text{m}} \cdot 0.55 \\ &= 2 \cdot R_\square \cdot \frac{l}{10\,\mu\text{m}} + 4.2 \cdot R_\square \end{aligned} \tag{3.2}$$

resulting in a length of $l = 1.036\,\text{mm}$ to achieve a unit cell of $R = 1\,\text{k}\Omega$. Higher resistances can be achieved by connecting several unit cells leading to big structures.

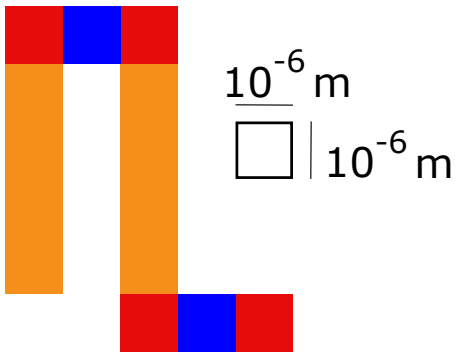


Fig. 21: A unit cell of the ohmic resistance of the ITO wire is shown. The corner pieces have sheet resistances of $0.55 \cdot R_\square$, whereas the other pieces have sheet resistances of $R_\square$.

Results
In table 7 the theoretically expected resistances R_{theo} and the actually created resistances R_{real} are shown, as well as the relative deviation ΔR. The relative deviation is less than 23 % for all resistances.

Tab. 7: The theoretically expected resistances R_{theo} calculated with eq. (3.2), the actually created resistances R_{real} and the relative deviation ΔR are shown.

$R_{\text{theo}}(\text{k}\Omega)$	$R_{\text{real}}(\text{k}\Omega)$	$\Delta R(\%)$
10	12.23	22.3
100	122.71	22.7
300	347.69	15.9
1000	1149.94	15.0

3.2.2 Switched Capacitor

Realisation
As high ohmic resistances take lots of space, they are unpractical in thin film technologies. However resistances can also be realized via switched capacitors as shown in fig. 22.

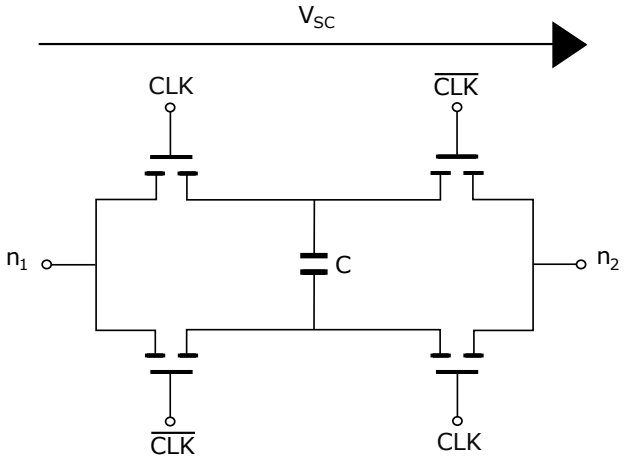


Fig. 22: The circuit design of a switched capacitor is shown. The capacity C is loaded alternating from V_{SC} to $-V_{\text{SC}}$ by four transistors. These are controlled by the clock (CLK) or anti-clock ($\overline{\text{CLK}}$) signal.

Four transistors are placed symmetrically around a capacity C and a clock (CLK) or anti-clock ($\overline{\text{CLK}}$) signal is applied to the gate of the transistors. The transistors placed diagonally to each other get the same clock signal. The capacity is charged alternating from V_{SC} to $-V_{\text{SC}}$ by the transistors. V_{SC} denotes the voltage between the nodes n_1 and n_2. By changing the frequency f_{SC} of the clock and anti-clock

signal, the resistance can be chosen, as

$$R_{\mathrm{SC}} = \frac{1}{4 \cdot C \cdot f_{\mathrm{SC}}} \tag{3.3}$$

holds [9]. Like this it is easy to achieve high resistances by using a low capacity and low frequencies to switch it. As low capacities are realized by plate capacitors with small areas, as seen in eq. (3.6), they can be realized without taking lots of space. Therefore they are favoured in thin film technology. A disadvantage of switched capacitors are the additional wires and signals needed to apply the clock and anti-clock frequency at the gates of the transistors. Moreover the switched capacitor works only as a resistance in the temporal average. Therefore the bandwidth for resistances realized by switched capacitors is $f_{\mathrm{SC}}/2$.

Results

To determine the resistance of the switched capacitor, a sinus signal with an amplitude of $V_{\mathrm{pp}} = 4\,\mathrm{V}$ was applied to an external resistor of $R = 60\,\mathrm{M\Omega}$. This signal was applied to the input of the switched capacitor and its output was connected to ground. Like this a voltage divider was created and the voltage drop at the switched capacitor V_{SC} was measured. The measuring setup is shown schematically in fig. 23.

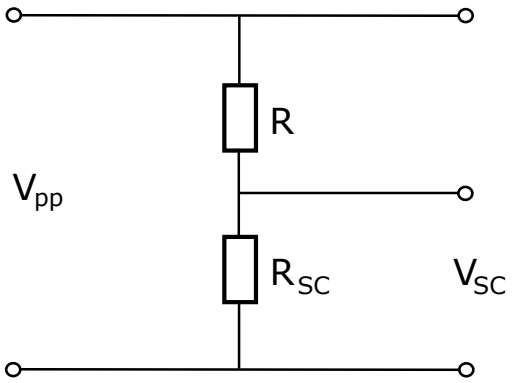


Fig. 23: The realized voltage divider to determine the resistance R_{SC} of the switched capacitor is shown.

The resistance could thus be calculated by

$$R_{\mathrm{SC}} = \frac{V_{\mathrm{SC}}}{V_{\mathrm{pp}} - V_{\mathrm{SC}}} \cdot 60\,\mathrm{M\Omega}. \tag{3.4}$$

Resistances up to $1.8\,\mathrm{G\Omega}$ could be achieved by applying low frequencies at the clock and anti-clock signal. The determined resistances for different frequencies of the clock and anti-clock signal are shown in fig. 24.

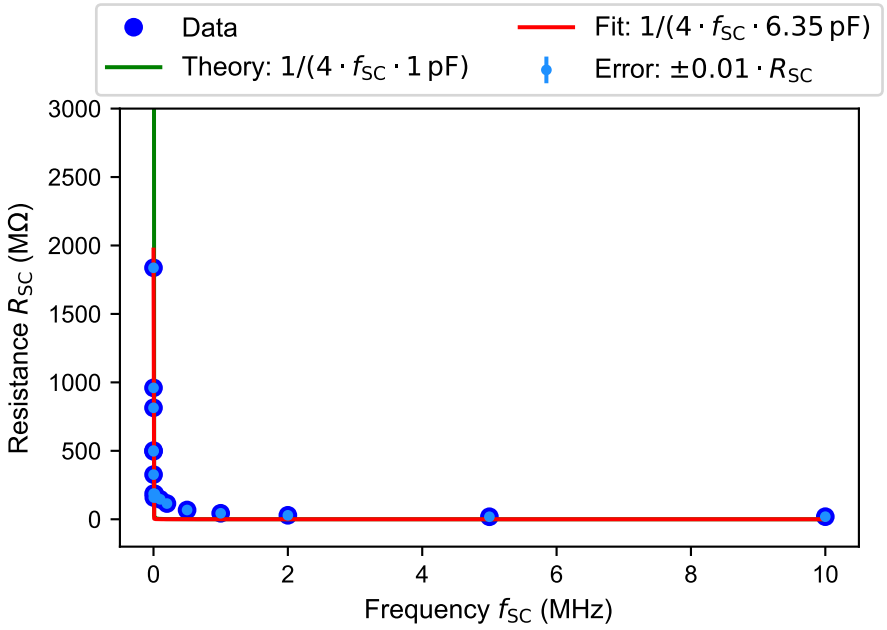


Fig. 24: The by eq. (3.4) determined resistances R_{SC} of the switched capacitor are shown as the blue dots for different frequencies f_{SC} of the clock and anti-clock signal. The green function refers to the theoretical dependency of eq. (3.3), where $C = 1\,\text{pF}$ was used, as realized in the examined switched capacitor. The red function is a fit function of eq. (3.3), where C was used as the fit parameter leading to $C_{\text{fit}} = 6.35\,\text{pF}$.

The blue dots refer to the determined data, whereas the green function shows the expected dependency of eq. (3.3) with $C = 1\,\text{pF}$ as produced. The red function is a fit function of the form of eq. (3.3), where C was used as a fit parameter leading to $C_{\text{fit}} = 6.35\,\text{pF}$. The two functions are nearly identical and match the data quite well. Only for frequencies where the functions have a high curvature, the data shows different behaviour as theoretically expected. This might be due to tolerance of the external resistance or inaccuracy during the measuring process. As external resistance six $10\,\text{M}\Omega$ resistors were connected in series. Each resistor has a tolerance of $\pm 1\,\%$. If all six resistors deviate in the same direction, the total deviation is maximal for the external resistance and $\Delta R = \pm 600\,\text{k}\Omega$ holds. The error of the determined resistances of the switched capacitor can be calculated to

$$\Delta R_{\text{SC}} = \left| \frac{V_{\text{SC}}}{V_{\text{pp}} - V_{\text{SC}}} \right| \cdot \Delta R = \pm 0.01 \cdot R_{\text{SC}} \tag{3.5}$$

using error correction. The errors are small compared to the absolute values of the resistance of the switched capacitor, which can be seen in fig. 24. Therefore the deviation between the data and the theoretical expectation can't be explained by the tolerance of the external resistor.

3.3 Capacities

Realisation

Capacities are realized by creating an overlap between the drain/source layer and the top gate layer. Like this a plate capacitor is created and the capacity can be specified by choosing the area of the overlap. The capacity C of a plate capacitor is defined as [13]

$$C = \epsilon_0 \cdot \epsilon_\mathrm{r} \cdot \frac{A_\mathrm{overlap}}{d} \quad , \tag{3.6}$$

where ϵ_0 is the electric field constant, ϵ_r the relative permittivity of the material, A_overlap the area of the overlap and d the distance between the two metal layers. As there is a dielectricum layer between the drain/source layer and the top gate layer, as explained in section 3.1, the distance between the plates of the capacitor equals the thickness of the dielectric layer. Hence $d = 130\,\mathrm{nm}$ holds. The relative permittivity was determined to $\epsilon_\mathrm{r} = 4.374$ using the theoretically expected and actually created capacities from [1]. The area of the overlap contains the overlap of the two plates and an additional overlap created by the wire of the top gate as seen in fig. 25. This wire is necessary as the width and the length of the drain/source layer are each $10\,\mu\mathrm{m}$ longer to prevent errors due to misalignment during the fabrication. The additional overlap has an area of $A_\mathrm{add} = 100 \cdot 10^{-12}\,\mathrm{m}^2$.

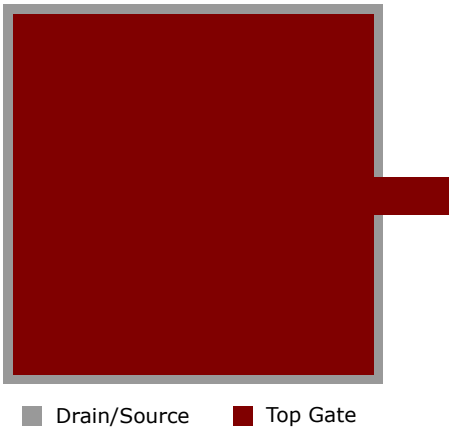


Fig. 25: The realized capacity as a plate capacitor between the drain/source and the top gate layer is shown.

Results

In table 8 the theoretically expected capacities C_theo, the average values of the actually created capacities $\overline{C_\mathrm{real}}$ and their relative deviation ΔC in dependence of the area A_overlap of the overlap are shown.

Tab. 8: The areas A_{overlap} of the overlap, as shown in fig. 25, are presented in dependency of the theoretically expected capacities C_{theo}, the average values of the actually created capacities $\overline{C_{\text{real}}}$ and their relative deviation ΔC.

C_{theo}(pF)	$A_{\text{overlap}}(10^{-9}\,\text{m}^2)$	$\overline{C_{\text{real}}}$(pF)	$\Delta C(\%)$
1	2.265	0.975	2.5
5	16.782	5.319	6.4
10	33.565	10.406	4.1

The relative deviation of the different capacities is less than 10 % for all capacities. The deviation can be explained by a different relative permittivity as determined or by a different overlap area due to misalignment during the fabrication.
Assuming that due to misalignment only the additional overlap area A_{add} changes, the error of the area is $\Delta A_{\text{overlap}} = \pm 100 \cdot 10^{-12}\,\text{m}^2$. If the top gate is aligned over the drain/source layer in a way, that the left edges are exactly over each other, the overlap is the biggest. If the right edges of the two layers are exactly over each other, the overlap is the smallest. The error of the produced capacities C_{produced} can be determined to

$$\Delta C_{\text{produced}} = \left| \epsilon_0 \cdot \epsilon_r \cdot \frac{1}{d} \right| \cdot \Delta A_{\text{overlap}} = \pm 0.030\,\text{pF} \tag{3.7}$$

using error propagation.
It can be seen that the additional overlap area due to misalignment has only small influence on the produced capacity. Therefore the deviation can be explained best by a different relative permittivity as calculated from previews realisations from [1].

4 Results

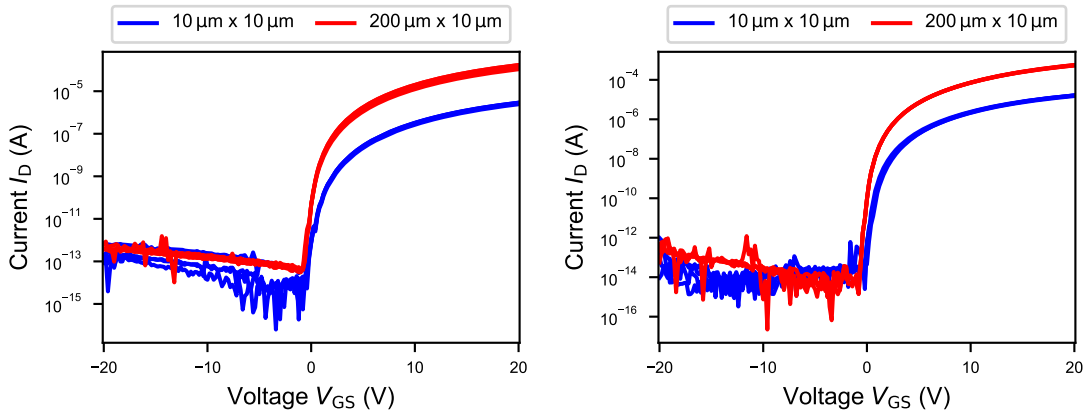
In the following the simulated circuits and the measurement results are discussed and compared.

4.1 Transistors

Transistors are the most used components in this work and therefore very important for the realisation of all produced analog and digital circuits. As the transistors are used as switches, the threshold voltage is an import magnitude to examine.

4.1.1 Transistors with different Channel Widths

TFTs with two different channel widths were produced and examined, one with a channel width of $w = 10\,\mu m$ and one with $w = 200\,\mu m$. The channel length is always $10\,\mu m$. On each substrate there are respectively four TFTs of each channel width. The drain source voltage was set to $10\,V$. By sweeping the gate source voltage V_{GS} between $-20\,V$ and $20\,V$ and measuring the drain current I_D, the characteristics were recorded. They are shown in blue for the TFTs for $w = 10\,\mu m$ and in red for $w = 200\,\mu m$ in fig. 26 for two different substrates.



(a) Substrate 2 (b) Substrate 3

Fig. 26: The characteristic between drain current I_D and gate source voltage V_{GS} is shown for respectively four TFTs with a channel width of $10\,\mu m$ in blue and a channel width of $200\,\mu m$ in red for different substrates. The drain source voltage was set to $10\,V$.

The characteristics for the different TFTs of the same channel width are nearly identical on each substrate. The TFTs with small channel widths have each different leakage currents in the cut-off region. The highest difference between the different leakage currents is around $9.9 \cdot 10^{-13}\,A$. As the highest leakage

current is still in the magnitude of pA, the TFTs are all still functional and won't behave very different. In comparison, the TFTs with large channel widths have even nearly identical leakage currents higher than those of the TFTs with smaller channel width.
Concerning the triode and saturation region, the TFTs with larger channel widths have higher drain currents as expected regarding eq. (2.3) and eq. (2.5). Therefore the slope in the triode region is higher for large channel widths and the resistance is lower as expected from eq. (2.4).

The TFTs of the different substrates have different drain currents in the saturation region. The drain current of the TFTs of the third substrate is one order of magnitude higher as the drain current of the TFTs of the second substrate. As the layout of each substrate is identical, the deviation of the drain currents of the same TFTs on different substrates is due to the production. The deposition of the semiconductor layer is non-uniform. On the second substrate, the semiconductor layer has an average thickness of 25.3 nm, whereas the semiconductor layer has an average thickness of 37.6 nm on the third substrate.

In table 9 the average threshold voltage and the average mobility of the charge carriers are shown for the TFTs with different channel widths for both substrates.

Tab. 9: The average threshold voltage $\overline{V_{\mathrm{th}}}$ and the average mobility $\overline{\mu}$ of the charge carriers is shown in dependence of the channel width w of the TFTs for the different substrates.

	Substrate 2		Substrate 3	
w(µm)	10	200	10	200
$\overline{V_{\mathrm{th}}}$(V)	5.67	5.43	4.55	4.41
$\overline{\mu}$	1.00	2.30	5.09	8.60

For both substrates the threshold voltage is lower for large channel widths. The threshold voltage of the TFTs with different channel widths on the same substrate only deviate in the magnitude of 200 mV. Therefore both types of TFTs need approximately the same voltage to get conductive. If the TFTs are used as switches as in this work, the TFTs with different channel widths will behave similar in circuits.
In comparison, the mobility of the charge carriers variates for the TFTs of different channel widths and of different substrates. It can be seen, that the mobility of the charge carriers is significantly higher for TFTs with larger channel widths. Moreover the mobility of the charge carriers is about four times higher for the third substrate. This corresponds to the observed higher drain current in the saturation region of the TFTs.

4.1.2 Phototransistors

To check the functionality of the four produced phototransistors on the substrate, the characteristic between drain current I_D and gate source voltage V_{GS} was recorded analogously to section 4.1.1. Additionally the characteristics were recorded while light of a microscope was applied to the phototransistors. In the microscope a halogen bulb with spectral parts in the ultraviolet is used.

In fig. 27 the characteristic with applied light is shown in red and without applied light in blue.

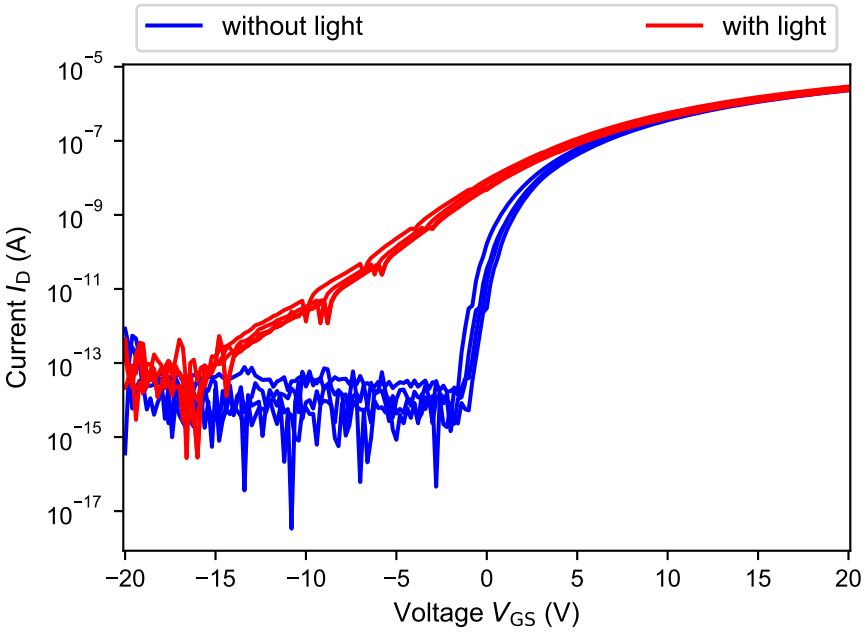


Fig. 27: The characteristics between drain current I_D and gate source voltage V_{GS} is shown for the realized phototransistors and a drain source voltage of 10 V. In red the characteristics with applied microscopy light and in blue the characteristics without applied light are shown.

Without applied light the characteristics correspond to the characteristics of the examined TFTs in section 4.1.1 and the transistors are functional in general. The characteristics change significantly for the applied microscopy light. In the cut-off region the drain current is no longer only the leakage current. Instead the current increases for voltages $V_{GS} > -15\,V$ as the transistor gets conductive because of the applied light. The photon energy of the ultraviolet parts of the microscopy light is high enough, so that the charge carriers can transcend the energy gap between valence and conductive band. Like this the functionality of the produced phototransistors is shown and they can be used to detect light.

4.2 Operational Amplifier

In the different track and hold circuits, opamps were used as buffers or as TIAs. Therefore it is important to check their functionality by looking at the frequency dependence of the gain and the phase. For the measurement a function generator was used to apply a sinus signal of different frequencies at the input. An additional external resistance of 10 MΩ was used to examine the TIA. The output signal was measured using an oscilloscope and an active probe.

4.2.1 Open Loop Configuration

In fig. 28 the Bode plot of the open loop configuration is shown. The gain G is determined using eq. (2.8) and is shown in blue. In red the phase P between input and output signal is shown.

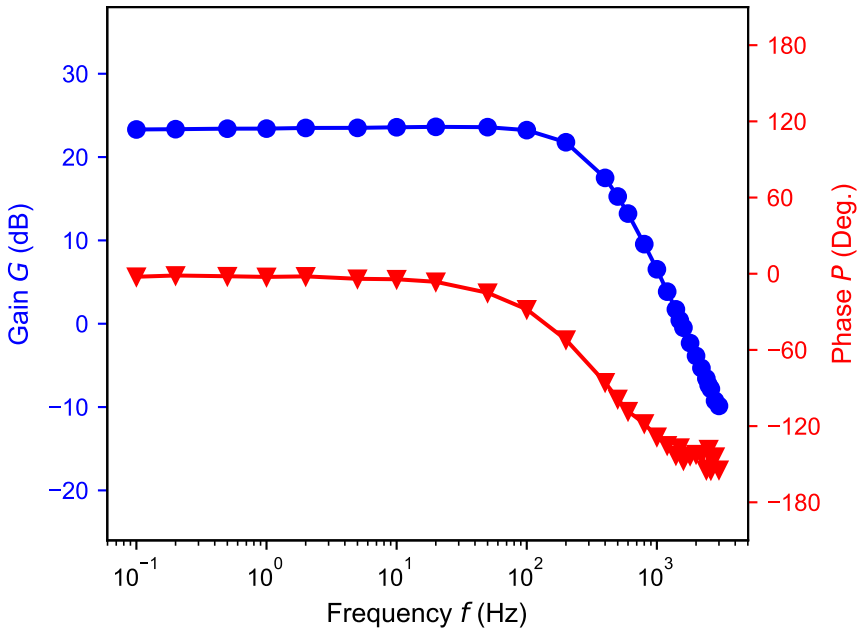


Fig. 28: The Bode plot of the open loop configuration is shown. In red the phase between input and output signal is presented and in blue the gain of the opamp is shown.

The bandwidth of the opamp can be determined to 283 Hz. For higher frequencies the gain decreases linearly with 20 dB/decade. For frequencies $f < 50$ Hz the phase only decreases very little and $P \approx 0°$ holds. For higher frequencies the phase decreases significantly and for a frequency $f \approx 1500$ Hz the phase is $P \approx -150°$. The Bode plot shows the expected characteristics and the open loop functionality of the opamp is verified.

4.2.2 Unity Gain Amplifier

In fig. 29 the Bode plot of the unity gain amplifier is shown. The phase between input and output is shown in red, whereas the gain is shown in blue.

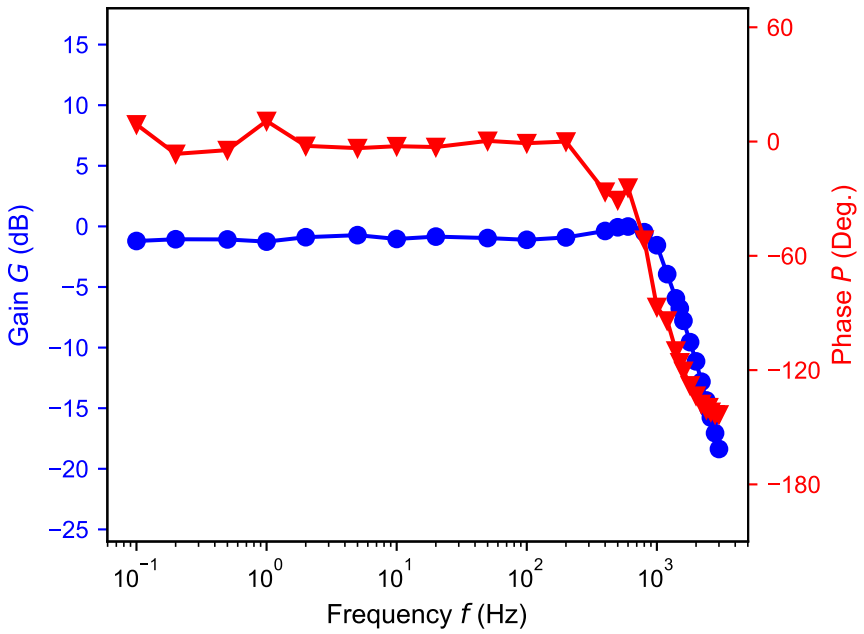
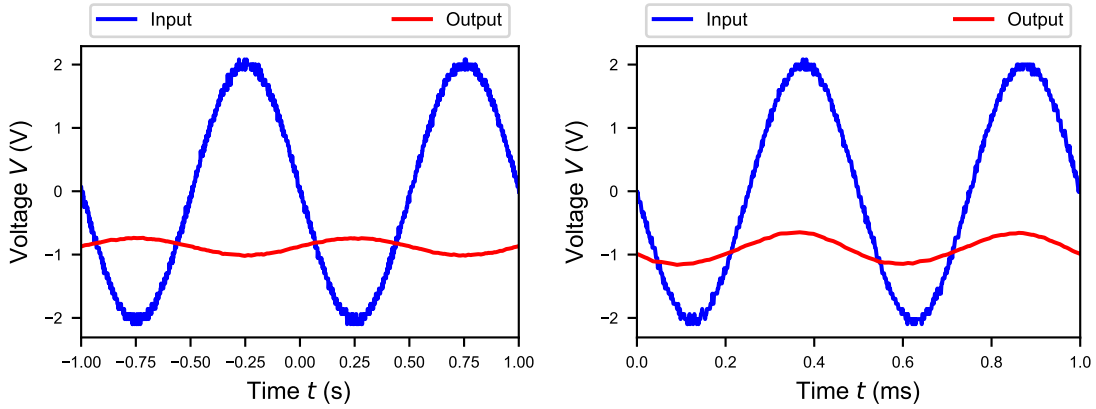


Fig. 29: The Bode plot of the unity gain amplifier is shown. In red the phase between input and output signal is presented and in blue the gain of the opamp is shown.

For frequencies $f < 1\,\mathrm{kHz}$ the gain is constant at $G \approx 0\,\mathrm{dB}$, as expected for the unity gain amplifier. For higher frequencies the gain decreases. The phase fluctuates for frequencies $f < 200\,\mathrm{Hz}$ around $P = 0°$. For higher frequencies a significant decrease is spotted.
Knowing these results, the unity gain amplifier should function well for frequencies $f < 1\,\mathrm{kHz}$. This is an important result concerning the track and hold circuits with buffers as the buffers are realized via unity gain amplifiers. Therefore a good behaviour concerning the tracking and holding phase is expected for frequencies $f < 1\,\mathrm{kHz}$.

4.2.3 Transimpedance Amplifier

TIAs were produced with ohmic resistances and with switched capacitors as feedback resistances.
In fig. 30 the input and output signal of the TIA with ohmic resistance is shown for different frequencies of the input signal. On the left the frequency is $f = 1\,\text{Hz}$ and on the right the frequency is $f = 2\,\text{kHz}$. The feedback resistance is $1\,\text{M}\Omega$.

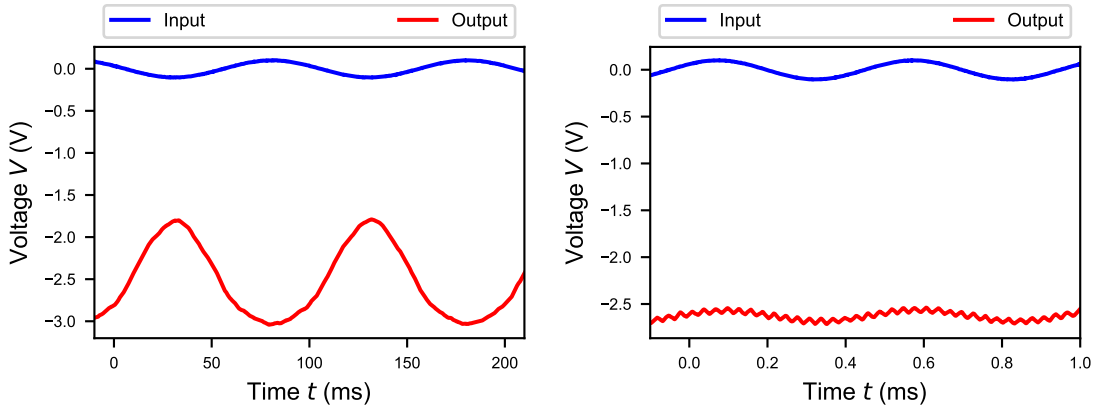


(a) $f = 1\,\text{Hz}$ (b) $f = 2\,\text{kHz}$

Fig. 30: The input signal applied to the TIA is shown in blue and the output signal is shown in red. On the left the input signal has a frequency of $f = 1\,\text{Hz}$, whereas the frequency of the input signal on the right is $f = 2\,\text{kHz}$. The feedback resistance of the TIA is an ohmic resistance of $1\,\text{M}\Omega$.

If an input signal with low frequency is applied, the output signal is inverted as expected for a TIA. For higher frequencies the phase between input and output signal shifts and at a frequency of $2\,\text{kHz}$ a phase shift of 180° is present. In this case the TIA is no longer functional, as the output is no longer inverted to the input signal. For frequencies in the magnitude of $100\,\text{Hz}$ the TIA is functional and the phase shift is only small.
It is noticeable that the TIA has a negative offset of approximately $1\,\text{V}$ for all frequencies applied. This will also have an influence on the track and hold circuit where TIAs are used to convert applied voltages to currents, which want to be detected. Moreover these circuits will only be functional for maximal frequencies in the magnitude of $100\,\text{Hz}$, as this is the range where the TIAs are functional.

In fig. 31 the measurements are shown for a TIA with switched capacitor as feedback resistance. In this case the feedback resistance is $15\,\text{M}\Omega$.



(a) $f = 1\,\mathrm{Hz}$ (b) $f = 2\,\mathrm{kHz}$

Fig. 31: The input signal applied to the TIA is shown in blue and the output signal is shown in red. On the left the input signal has a frequency of $f = 1\,\mathrm{Hz}$, whereas the frequency of the input signal on the right is $f = 2\,\mathrm{kHz}$. The feedback resistance of the TIA is $15\,\mathrm{M\Omega}$ and it is realized with a switched capacitor.

As for the TIA with ohmic feedback resistance, the functionality can be shown for small frequencies. At a frequency of $2\,\mathrm{kHz}$ a phase shif of 180° is present as seen for the TIA with ohmic feedback resistance. However the offset is approximately $-2.5\,\mathrm{V}$ and a decrease of the amplitude of the output signal can be seen for increasing frequency. Therefore the bandwidth of the TIA with switched capacitor is smaller.
Knowing these results, the use of TIAs with ohmic resistances as feedback resistances is favourable.

4.3 Track and Hold Circuits with Input Voltage

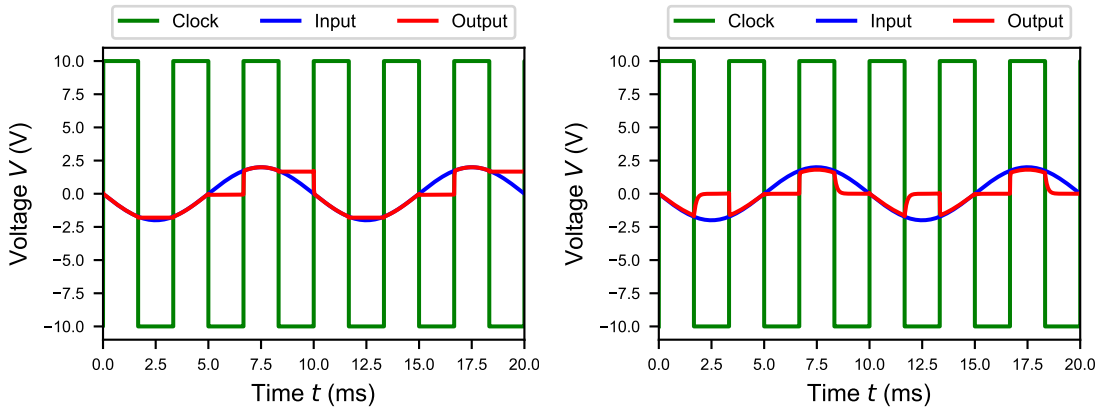
Track and hold circuits are able to track and hold input voltages. Like this it is possible to read out a signal at a later time. The different track and hold circuits explained in section 2.5 were examined for different frequencies. First the circuits were simulated using `AIM-Spice` and then they were measured. Therefore a sinus signal with $-2\,\mathrm{V} \leq V \leq 2\,\mathrm{V}$ and frequency f was applied as input signal of the circuit. At the gate of the transistor a square function with $-10\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and a frequency of $3f$ was applied. The output signal was recorded by an oscilloscope with active probe.

4.3.1 Track and Hold Circuit consisting of a Transistor and a Capacity

The easiest track and hold circuit is the track and hold circuit with one transistor and one capacity.

Simulation

In fig. 32 the simulated track and hold circuit is shown. If the signal at the gate of the transistor is high, the input signal is tracked and the input signal and the output signal are identical. In comparison if the signal at the gate of the transistor is low, the input signal is held and the output signal corresponds to the input signal of the last tracking phase. The output signal stays constant during the whole holding phase for an ideal track and hold circuit as simulated.



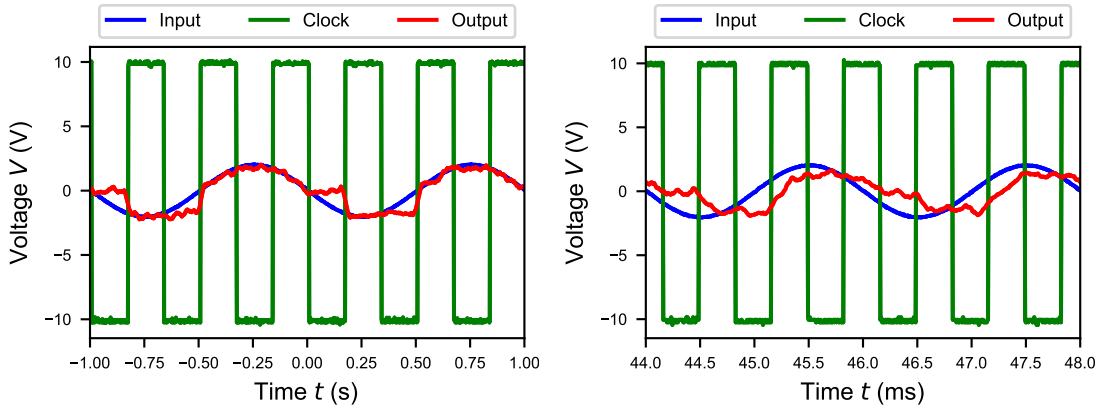
(a) without oscilloscope (b) with oscilloscope

Fig. 32: The input signal of the track and hold circuit is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green. On the left the input of the oscilloscope was not considered in the simulation and on the right it was considered.

If the oscilloscope was simulated at the end of the track and hold circuit, the output signal changes significantly for the holding phases. The held signals are all zero, which can be seen in fig. 32 on the right. It can be seen, that the held signals correspond to the tracked signals at the beginning of the holding phase. Then the held signal gets discharged by the oscilloscope used to record the output signal. This could be avoided by adding an output buffer to the track and hold circuit.

Measurement Result

In fig. 33 the input, output and clock signal at the gate of the transistor are shown for the measured track and hold circuit. On the left a frequency of $f = 1\,\mathrm{Hz}$ was chosen and on the right the frequency is $f = 500\,\mathrm{Hz}$.



(a) $f = 1\,\mathrm{Hz}$ (b) $f = 500\,\mathrm{Hz}$

Fig. 33: The input signal of the track and hold circuit is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

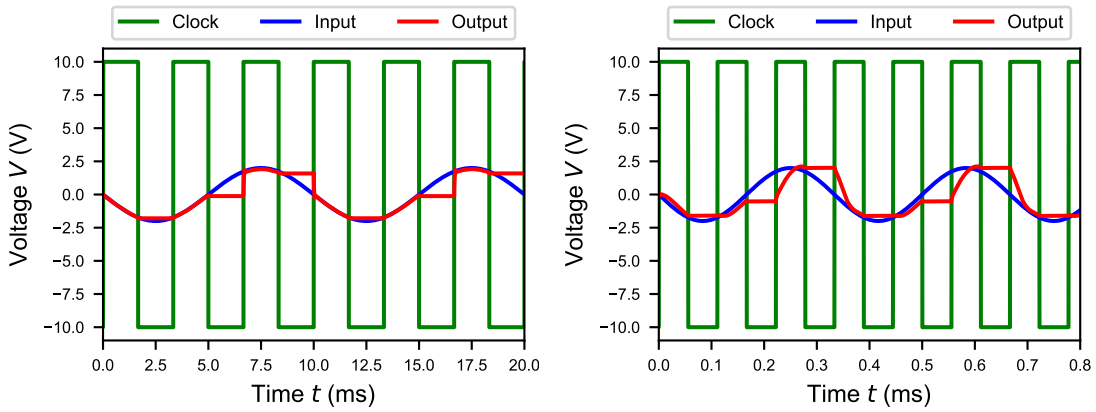
In comparison to the simulated circuit with oscilloscope, the held signal corresponds to the tracked one. This can be explained by the used active probe at the oscilloscope, which decouples the signals and avoids that the held signal is discharged by the oscilloscope. Nevertheless it is noticeable, that the held signal is not constant. On the one hand there is noise due to the measurement setup and on the other hand the held signals decrease or increase when the gate signal switches from high to low or from low to high. This can be explained by the crosstalk between the different signals.
The circuit works well for frequencies $f < 500\,\mathrm{Hz}$. For higher frequencies the tracked signal is not identical with the input signal, as the tracking phase is to short to charge the capacity to the input signal. Therefore the held signal does not correspond to the signal that should have been tracked.

4.3.2 Track and Hold Circuit with Input Buffer

By adding an input buffer to the track and hold circuit, the held signal should be improved as explained in section 2.5.2.

Simulation
Like for the track and hold circuit consisting of a transistor and a capacity described in section 4.3.1, the held signal gets discharged by the oscilloscope and therefore the circuit is not working, if the oscilloscope is simulated. In fig. 34 the simulated track and hold circuit with input buffer and without oscilloscope is shown. It can be seen, that the capacity charges and discharges in a shorter time as expected for the use of an input buffer. Moreover it can be seen, that for a frequency of 3 kHz nearly the whole tracking phase is needed to reach the input signal. Therefore the circuit won't be functional for even higher frequencies, as

the tracked signal does not correspond to the input signal.

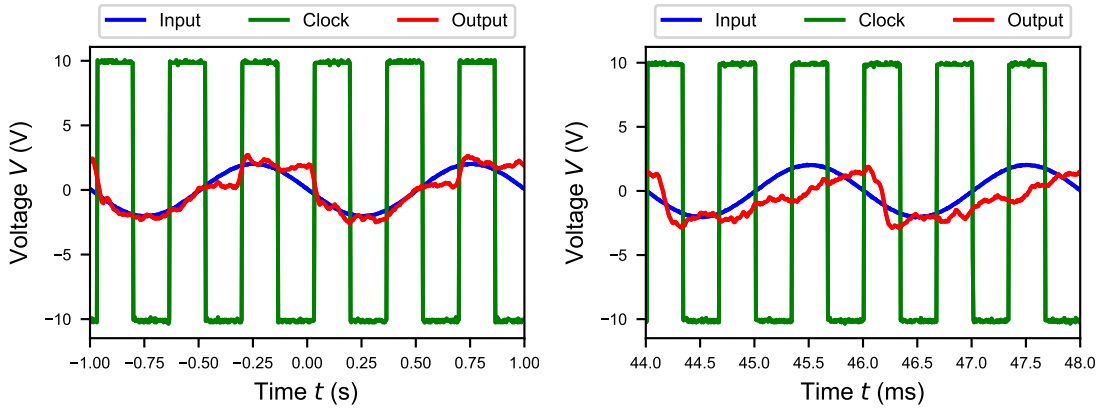


(a) $f = 100\,\text{Hz}$ (b) $f = 3\,\text{kHz}$

Fig. 34: The input signal of the track and hold circuit with input buffer is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

Measurement Results

In fig. 35 the input, output and clock signal at the gate of the transistor are shown for the measured track and hold circuit with input buffer. On the left a frequency of $f = 1\,\text{Hz}$ was chosen and on the right the frequency is $f = 500\,\text{Hz}$.



(a) $f = 1\,\text{Hz}$ (b) $f = 500\,\text{Hz}$

Fig. 35: The input signal of the track and hold circuit with input buffer is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

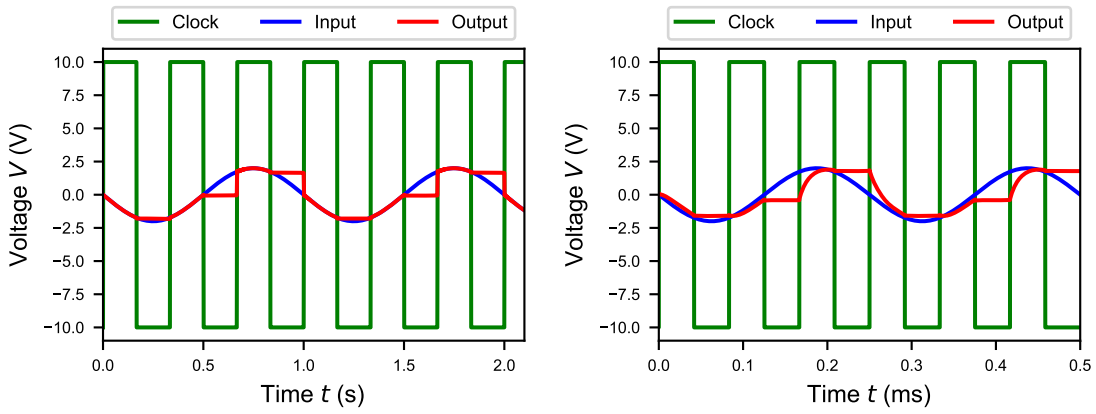
As for the track and hold circuit consisting of a transistor and a capacity, the held signal corresponds to the tracked one for the measured circuit due to the used

active probe. However the held signal is more constant as for the track and hold circuit consisting of a transistor and a capacity, which can be explained by the used input buffer.
At a frequency of 500 Hz the circuit is not functional anymore as the tracked signal and the input signal aren't identical anymore. The critical frequency is much lower as simulated. This can be explained by the additional parasitic capacities and resistances in the real circuit with measurement setup.

4.3.3 Track and Hold Circuit with Output Buffer

According to section 2.5.3 the held output signal should not be discharged by the oscilloscope when adding an output buffer to the track and hold circuit.

Simulation
In fig. 36 the simulated track and hold circuit with output buffer is shown for a frequency of 1 Hz on the left and for a frequency of 4 kHz on the right.



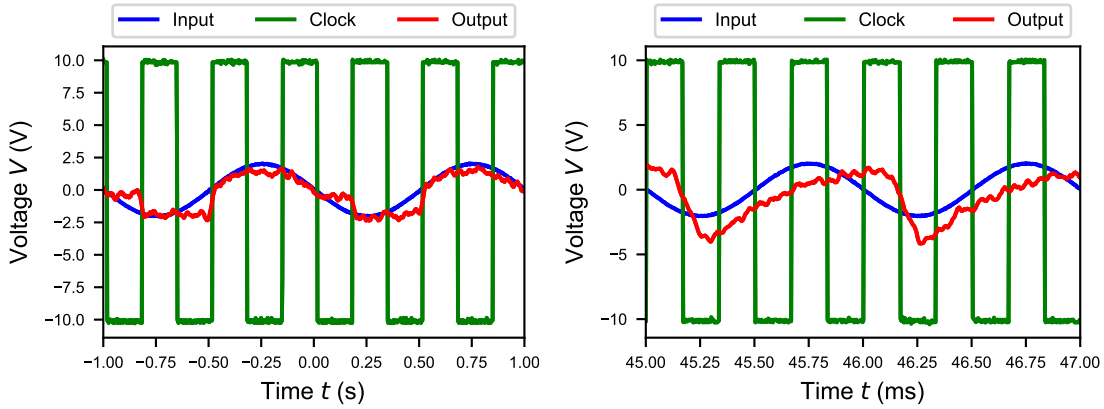
(a) $f = 1\,\text{Hz}$ (b) $f = 4\,\text{kHz}$

Fig. 36: The input signal of the track and hold circuit with output buffer is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

It can be seen that the circuit is fully functional for small frequencies. The held signal is constant and is not discharged by the oscilloscope because of the low output resistance of the output buffer.
For a frequency of 4 kHz the tracked signal needs the whole tracking phase to reach the input signal. For even higher frequencies this circuit won't be functional anymore as the input signal can't be tracked during the tracking phase.

Measurement Results
In fig. 37 the input, output and clock signal at the gate of the transistor are shown for the measured track and hold circuit with output buffer and a capacity of 10 pF.

On the left a frequency of $f = 1\,\text{Hz}$ was chosen and on the right the frequency is $f = 1\,\text{kHz}$.

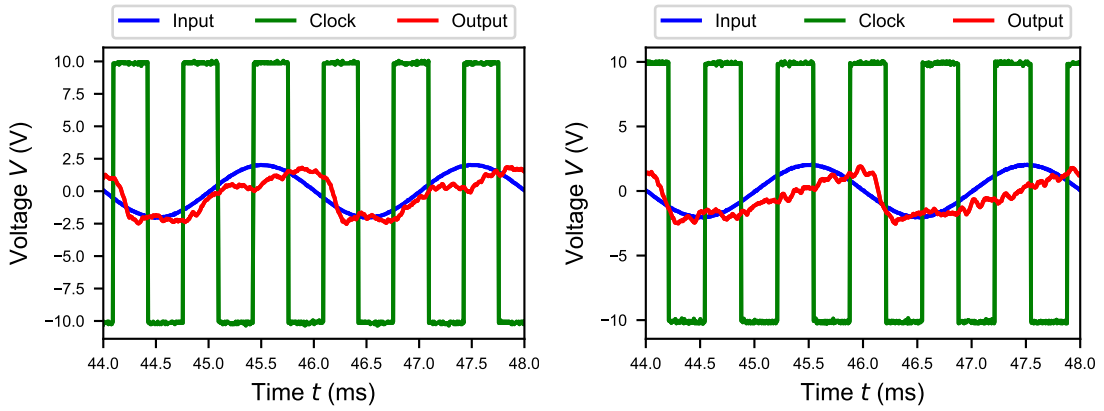


(a) $f = 1\,\text{Hz}$ (b) $f = 1\,\text{kHz}$

Fig. 37: The input signal of the track and hold circuit with output buffer and a capacity of 10 pF is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

For small frequencies the circuit is fully functional and corresponds to the simulated one. Due to the measurement setup the critical frequency is reached at 1 kHz and not at 4 kHz as expected after the simulation.

For this circuit the chosen capacity of the track and hold circuit has an influence. This can be seen best at a frequency of 500 Hz as shown in fig. 38.



(a) $C = 10\,\text{pF}$ (b) $C = 5\,\text{pF}$

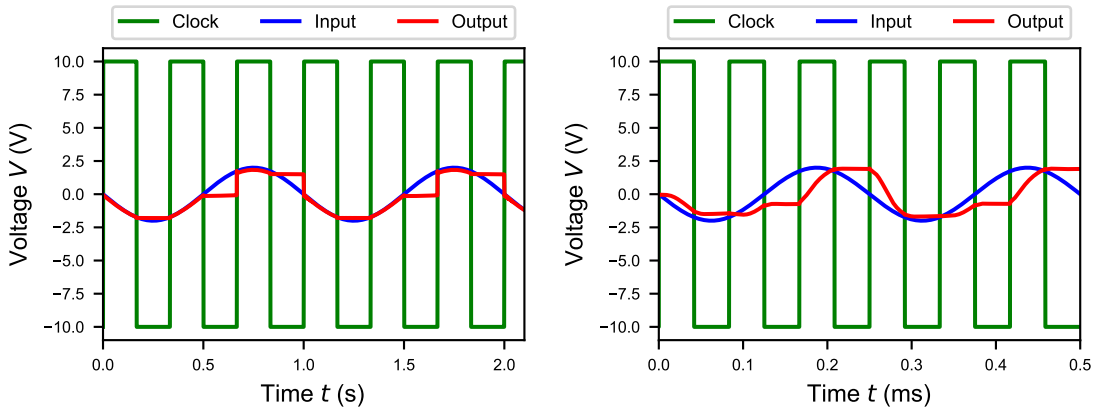
Fig. 38: The input signal of the track and hold circuit with output buffer and a frequency of 500 Hz is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different capacities C.

For a capacity of 10 pF the tracked signal corresponds still to the input signal most of the time and the held signal is constant. In comparison for a capacity of 5 pF the output signal looks like a triangular signal and the circuit s not functional anymore. Therefore the use of a capacity of 10 pF is favourable.

4.3.4 Track and Hold Circuit with Input Buffer and Output Buffer

By using a track and hold circuit with input buffer and output buffer, the capacity should be charged quickly and should not be discharged by the oscilloscope as explained in section 2.5.4.

Simulation
In fig. 39 the simulated track and hold circuit with input buffer and output buffer is shown for a frequency of 1 Hz on the left and for a frequency of 4 kHz on the right.

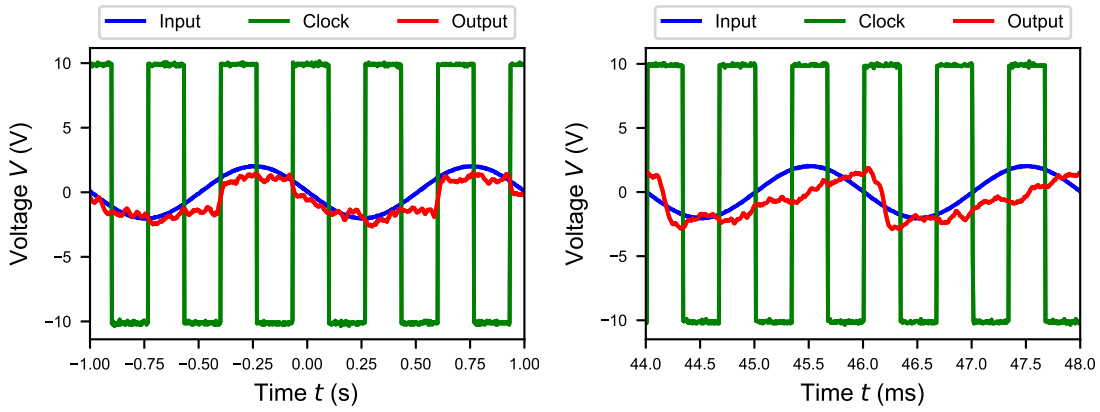


(a) $f = 1\,\text{Hz}$ (b) $f = 4\,\text{kHz}$

Fig. 39: The input signal of the track and hold circuit with input buffer and output buffer is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

For frequencies $f < 4\,\text{kHz}$ the circuit is functional as the tracked signal corresponds to the input signal and the held signal is constant. In comparison to the track and hold circuit with output buffer shown in fig. 36, the held signals are not as constant for this circuit. This does not correspond to the expectation, whereby the combination of input buffer and output buffer should be favourable. However this corresponds to the results of the simulation of the input buffer. For the circuit with input buffer and high frequencies, the held signal is not constant. Therefore the held signal in the circuit with input buffer and output buffer is also influenced by the input buffer and a track and hold circuit with output buffer is the best choice.

Measurement Results
In fig. 40 the input, output and clock signal at the gate of the transistor are shown for the measured track and hold circuit with input buffer and output buffer. On the left a frequency of $f = 1\,\text{Hz}$ was chosen and on the right the frequency is $f = 500\,\text{Hz}$.



(a) $f = 1\,\text{Hz}$ (b) $f = 500\,\text{Hz}$

Fig. 40: The input signal of the track and hold circuit with input buffer and output buffer is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

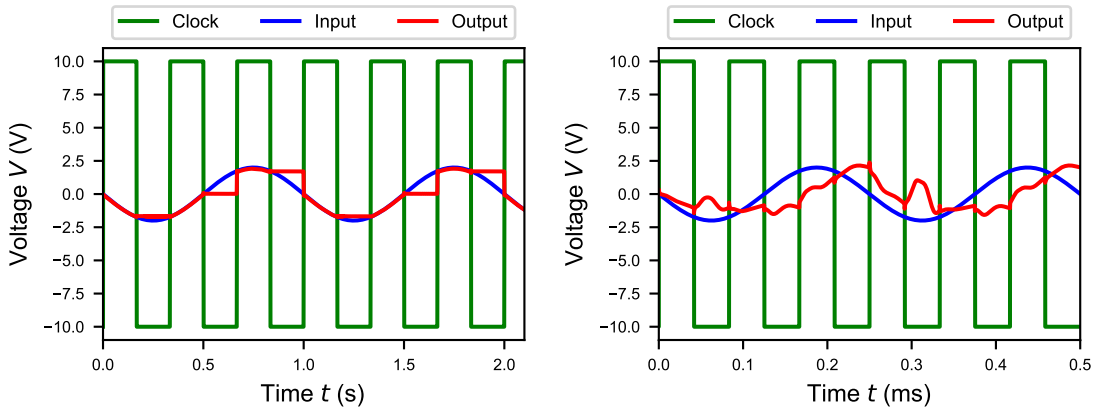
It can be seen that the circuit is functional for small frequencies. At a frequency of 500 Hz the output signal resembles a triangular signal and the track and hold circuit is not functional anymore. As the track and hold circuit with output buffer is functional for a larger bandwidth, it is favourable to use this circuit instead of the one with input buffer and output buffer.

4.3.5 Track and Hold Circuit with Miller Capacity

Track and hold circuits with Miller capacities should work best, as different capacities in the tracking and holding phase are used to optimize the output signal. This is explicitly described in section 2.5.5.

Simulation
In fig. 41 the simulated track and hold circuit with Miller capacity is shown for a frequency of 1 Hz on the left and for a frequency of 4 kHz on the right. Like for the different types of track and hold circuits, this circuit is fully functional for small frequencies. At a frequency of 4 kHz the tracked signal and the input signal are not identical and therefore the circuit is not functional anymore. Moreover the held signals are not constant. In comparison to the output signal of the track and hold circuit with output buffer shown in fig. 36, the tracked and held signal

is much worse at higher frequencies. Therefore the track and hold circuit with output buffer is favourable to use.

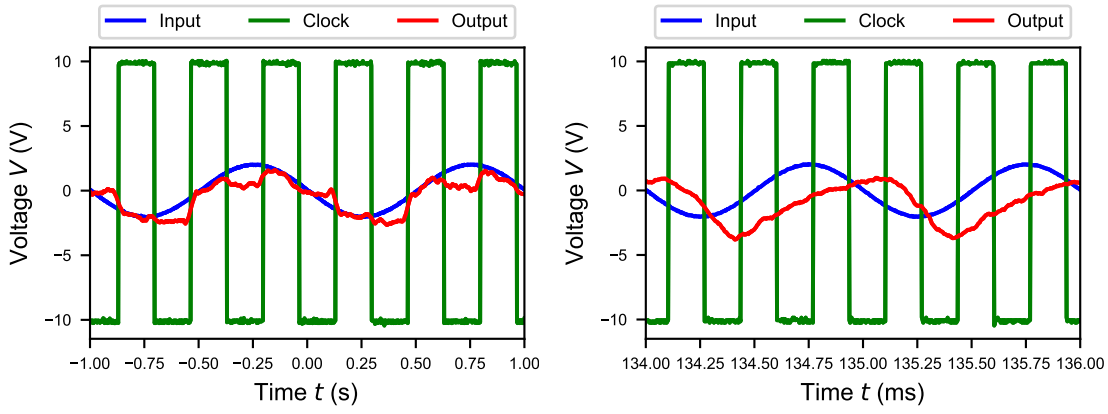


(a) $f = 1\,\mathrm{Hz}$ (b) $f = 4\,\mathrm{kHz}$

Fig. 41: The input signal of the track and hold circuit with Miller capacity is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

Measurement Results

Concerning the measurement results the track and hold circuit with Miller capacity and the track and hold circuit with output buffer are similar. In fig. 42 the input, output and clock signal at the gate of the transistor are shown for the measured track and hold circuit with Miller capacity. On the left a frequency of $f = 1\,\mathrm{Hz}$ was chosen and on the right the frequency is $f = 1\,\mathrm{kHz}$.



(a) $f = 1\,\mathrm{Hz}$ (b) $f = 1\,\mathrm{kHz}$

Fig. 42: The input signal of the track and hold circuit with Miller capacity is shown in blue, the output signal in red and the clock signal at the gate of the transistor in green for different frequencies f.

For frequencies $f < 1\,\text{kHz}$ the circuit is functional and for higher frequencies the tracked signal does not correspond to the input signal. In comparison to the other track and hod circuits an improvement of the holding phase, like theoretically expected, can't be seen. As the results are similar for the track and hold circuit with output buffer and this circuit is not as complicated as the circuit with the Miller capacity, the track and hold circuit with output buffer is the best circuit to use.

4.3.6 Holding Phase for different Capacities

The holding phase is very important for track and hold circuits. The held signal has to be constant while the signal is read out. As track and hold circuits can be used as pixels in arrays, it takes some time to read them out. During this time the held signal has to stay constant in order to not create errors. Therefore it is important to achieve track and hold circuits with constant held signals.

The quality of the holding phase can be modified by choosing different capacities in the track and hold circuit. During this work a capacity of 5 pF and one of 10 pF were chosen. To examine the holding phase, track and hold circuits with output buffers and the two different capacities were used. It is important to use track and hold circuits with output buffers, because otherwise the capacity would be discharged by the oscilloscope used to record the holding phase. The potential at the gate of the transistor was first set high so that the circuit was in the tracking phase. During this time the input signal was turned on and then the potential at the gate of the transistor was set low. By setting the potential at the gate of the transistor low, the circuit was in the holding phase. The whole process was recorded by the oscilloscope and is shown in fig. 43. The potential at the gate of the transistor is shown in green and the input signal is shown in blue. The tracked and held signal is shown in red for the capacity of 5 pF and in orange for the capacity of 10 pF.

For both capacities it is noticeable that the held signal decreases with time. However the curves differ strongly. Whereas the held signal of the circuit with the high capacity only decreases slightly, the decrease of the circuit with the low capacity is larger in comparison. The held signal for the capacity of 10 pF decreases by 2.85 V, while the held signal for a capacity of 5 pF decreases by 8.24 V in a timespan of 450 s. Moreover the held signal even gets negative for the low capacity and seems to reach the gate source voltage of $-5\,\text{V}$. This can be explained by the leakage currents of the used TFTs. As seen in fig. 26 in the cut-off region of the TFTs leakage currents are present charging the capacity. As the leakage currents are only very small, the charging process is slow. For a higher capacity the time constant is also higher leading to a slower discharging process of the capacity. Like this the held signal decreases slighter for high capacities.

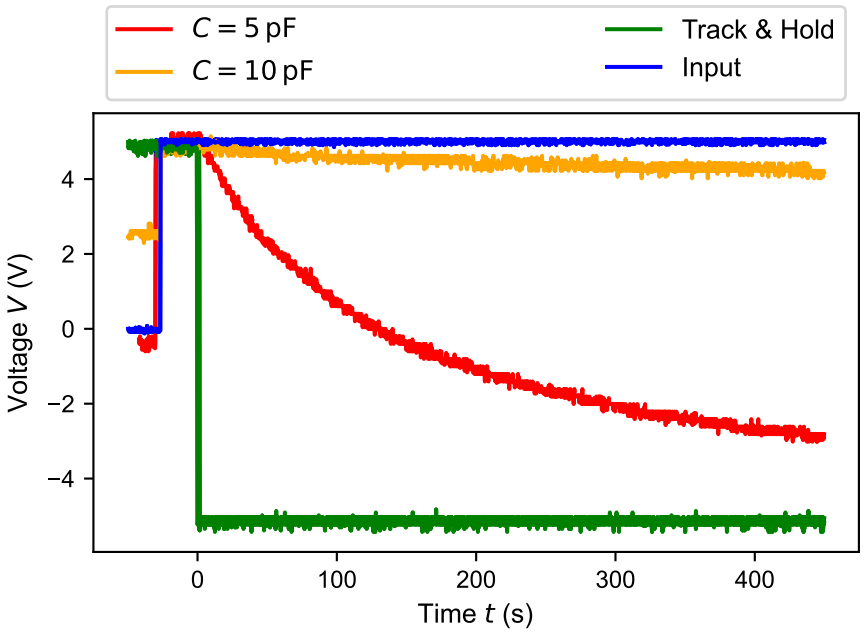


Fig. 43: The holding phase of the track and hold circuit with output buffer is shown in red for a capacity of 5 pF and in orange for a capacity of 10 pF. In blue the input signal and in green the signal at the gate of the transistor is shown.

As the held signal is much more constant using a capacity of 10 pF, it is reasonable to use this capacity in the track and hold circuits, especially when using them as array pixels. Nevertheless the read-out process of the pixels is in the magnitude of ms and therefore the use of capacities of 5 pF also works.

4.4 Track and Hold Circuits with Input Current

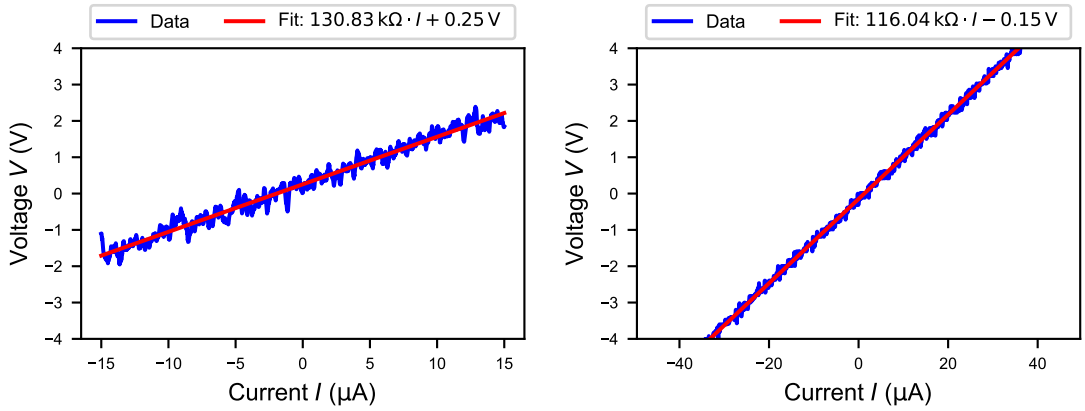
Phototransistors can be used to detect light intensities. High light intensities lead to high drain currents and low light intensities lead to low drain currents. However track and hold circuits need input voltages. Thus devices converting currents to voltages, like resistances or TIAs are needed to measure currents with track and hold circuits.

4.4.1 Track and Hold Circuits with Ohmic Resistance

A simple way to convert currents into voltages is the use of ohmic resistances. A resistance of 100 kΩ was placed in front of the track and hold circuits explained in section 2.5. These circuits were all realized on the same substrate, including the resistances.
To examine the circuits a current was applied as input of the track and hold circuits. The current was swept in suitable ranges for the different possible circuits and the output of the track and hold circuit was measured using an

oscilloscope with active probe. At the gate of the transistor a square function with $0\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and a frequency of 0.5 Hz was applied.

Track and Hold Circuit consisting of a Transistor and a Capacity
In fig. 44 the output signal of the track and hold circuits with capacities of 5 pF and 10 pF are shown in blue. Moreover linear functions were fitted to the data and are shown in red. For the capacity of 5 pF, the current was swept for $-15\,\mu\mathrm{A} \leq I \leq 15\,\mu\mathrm{A}$ and for the capacity of 10 pF for $-45\,\mu\mathrm{A} \leq I \leq 45\,\mu\mathrm{A}$.



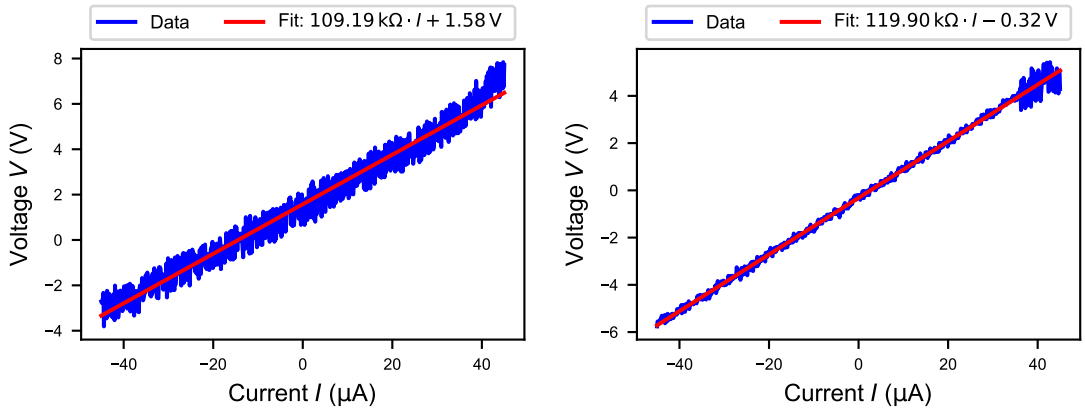
(a) $C = 5\,\mathrm{pF}$ (b) $C = 10\,\mathrm{pF}$

Fig. 44: The measured output signal of the track and hold circuit for an input current sweep is shown in blue. A linear function is fitted to the data and shown in red. On the left the capacity of the track and hold circuit is $C = 5\,\mathrm{pF}$ and on the right $C = 10\,\mathrm{pF}$.

For both capacities the functionality of the track and hold circuit in the chosen current range can be seen. The tracking phases can be seen as the peaks above the fit function, whereas the dips below the fit function correspond to the holding phases. By comparing the output signals of the circuits with different capacities, it is noticeable that the dips and peaks are larger for the capacity of 5 pF. This corresponds to the result of section 4.3.6. The held signal decreases faster for small capacities and therefore the dips are deeper for the same timespan.
The slope of the fit function corresponds to the ohmic resistance of the circuit. For the capacity of 5 pF a resistance of 130.83 kΩ can be determined and for the capacity of 10 pF a resistance of 116.04 kΩ results. In theory a resistance of 100 kΩ was produced, but as seen in table 7, the actually created resistance is 122.71 kΩ on average. Therefore the determined resistances correspond well and the produced circuits are functional.

Track and Hold Circuit with Input Buffer
In fig. 45 the output signals of the track and hold circuits with input buffer are shown in blue for the different ohmic resistances. The input currents were swept for $-45\,\mu\mathrm{A} \leq I \leq 45\,\mu\mathrm{A}$. Additionally linear functions were fitted to the data and are

shown in red. Thereby the ohmic resistances are determined to $R = 109.19\,\mathrm{k\Omega}$ for the capacity of 5 pF and $R = 119.90\,\mathrm{k\Omega}$ for the capacity of 10 pF. This corresponds to the expected value.



(a) $C = 5\,\mathrm{pF}$ (b) $C = 10\,\mathrm{pF}$

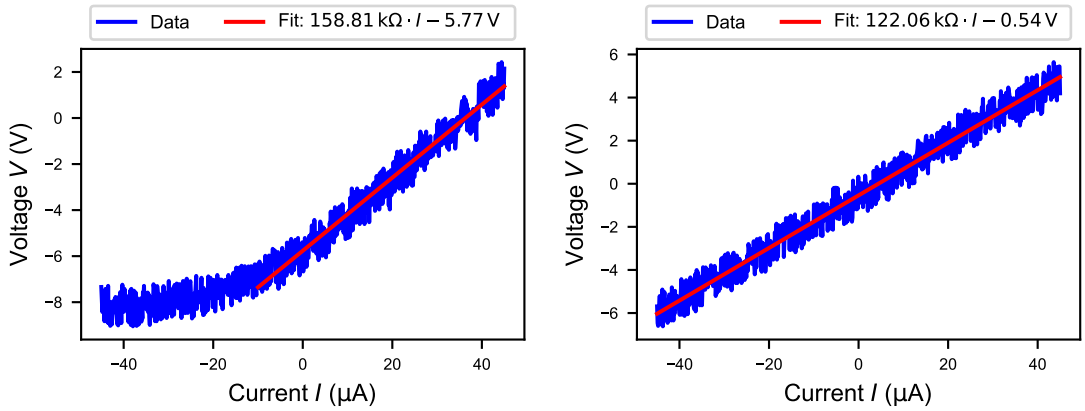
Fig. 45: The measured output signal of the track and hold circuit with input buffer for an input current sweep is shown in blue. A linear function is fitted to the data and shown in red. On the left the capacity of the track and hold circuit is $C = 5\,\mathrm{pF}$ and on the right $C = 10\,\mathrm{pF}$.

Track and Hold Circuit with Output Buffer

In fig. 46 the output signals of the track and hold circuits with output buffers are shown for swept input currents $-45\,\mu\mathrm{A} \leq I \leq 45\,\mu\mathrm{A}$ and the different ohmic resistances. A linear function was fitted to the data and is shown in red.

For a capacity of 10 pF the output voltage depends linearly on the input voltage as expected. Instead for the capacity of 5 pF the behaviour is different. For currents $I > -10\,\mu\mathrm{A}$ a linear dependency is present, whereas for smaller currents the voltage approaches asymptotically $-9\,\mathrm{V}$. This can be explained by the used output buffer. For small currents the output voltage would be lower than the negative supply voltage of the output buffer. As the output of opamps are limited by the supply voltages, the output voltage of the track and hold circuit approaches the supply voltage and gets in the rail.

The ohmic resistances can be determined to $R = 158.81\,\mathrm{k\Omega}$ for a capacity of 5 pF and to $R = 122.06\,\mathrm{k\Omega}$ for a capacity of 10 pF. For the higher capacity the resistance corresponds well to the expected value, whereas for the lower capacity the resistance differs.



(a) $C = 5\,\mathrm{pF}$ (b) $C = 10\,\mathrm{pF}$

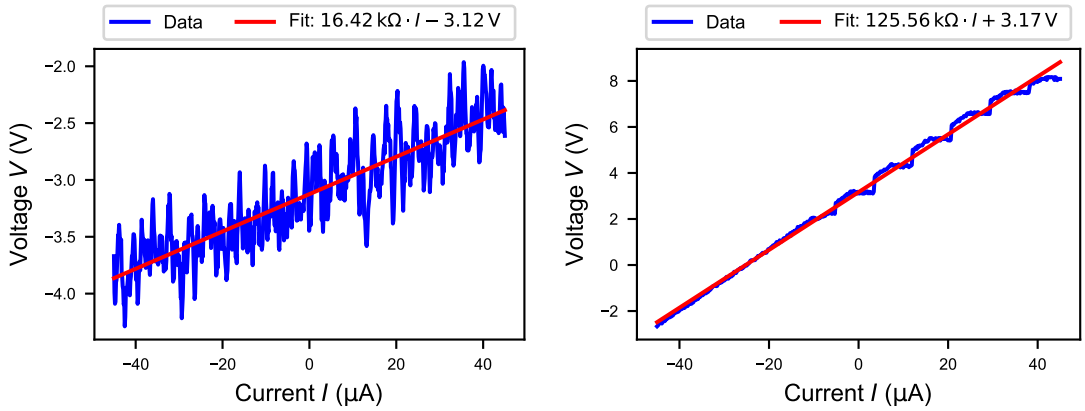
Fig. 46: The measured output signal of the track and hold circuit with output buffer for an input current sweep is shown in blue. A linear function is fitted to the data and shown in red. On the left the capacity of the track and hold circuit is $C = 5\,\mathrm{pF}$ and on the right $C = 10\,\mathrm{pF}$.

In general both circuits are functional. As the circuit with a capacity of 5 pF has a high absolute input offset of $-5.77\,\mathrm{V}$, it is favourable to use the circuit with the higher capacity.

Track and Hold Circuit with Input Buffer and Output Buffer

In fig. 47 the output signal of the track and hold circuit with input buffer and output buffer are shown in blue. A linear function was fitted to the data and is shown in red.

For both capacities a linear dependency between the output voltage and the input current can be seen. The ohmic resistances can be determined to $R = 16.42\,\mathrm{k\Omega}$ for a capacity of 5 pF and to $R = 125.56\,\mathrm{k\Omega}$ for a capacity of 10 pF. The resistance for the low capacity does not correspond to the expected value. On the one hand it is possible, that the used ohmic resistor is not so functional due to production errors. On the other hand it is possible, that the circuit in general is not so functional as the total resistance is too low. As the low resistance results in only small voltage changes for current changes, it is not favourable to use this circuit in combination with phototransistors. However the track and hold circuit with input buffer and output buffer and a capacity of 10 pF can be used as it is functional. Both circuits have high offsets and therefore these circuits are not favourable to use in general.



(a) $C = 5\,\mathrm{pF}$ (b) $C = 10\,\mathrm{pF}$

Fig. 47: The measured output signal of the track and hold circuit with input buffer and output buffer for an input current sweep is shown in blue. A linear function is fitted to the data and shown in red. On the left the capacity of the track and hold circuit is $C = 5\,\mathrm{pF}$ and on the right $C = 10\,\mathrm{pF}$.

Track and Hold Circuit with Miller Capacity

In fig. 48 the output signal of the track and hold circuit with Miller capacity is shown in blue. Moreover a linear function was fitted to the data and is shown in red.

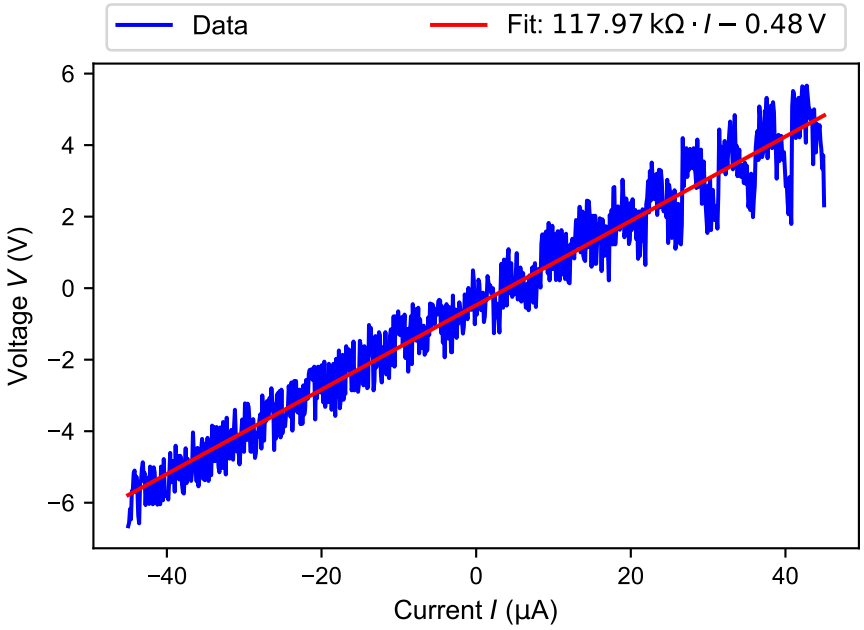


Fig. 48: The measured output signal of the track and hold circuit with Miller capacity is shown in blue. In red a linear fit function is shown.

The output voltage of the track and hold circuit increases linearly with increasing input current. As the slope of the fit function corresponds to the ohmic resistance of the circuit, $R = 117.97\,\mathrm{k\Omega}$ results. The determined ohmic resistance corresponds well to the expected one.
The track and hold phases can be seen as peaks and dips of the voltage. For high input currents the held signal decreases significantly and therefore it is favourable to use this circuit for lower input currents.

4.4.2 Track and Hold Circuits with Switched Capacitor

Resistances realized by switched capacitors can also be used to convert currents into voltages and can therefore be used in track and hold circuits. An advantage of these resistances is that the resistance can be varied by changing the clock and anti-clock frequency. Like that the magnitude of the voltage in dependence of the input current can be changed easily.

To check the functionality of the different track and hold circuits with switched capacitors as resistances to convert input currents, an input sinus signal with $-400\,\mathrm{mV} \leq V \leq 400\,\mathrm{mV}$ was applied through an external resistor of $10\,\mathrm{M\Omega}$ at the input of the circuit. At the gate of the transistor a square function with $-7\,\mathrm{V} \leq V \leq 7\,\mathrm{V}$ was applied as track and hold signal and the output signal of the circuit was recorded by an oscilloscope with active probe. Additionally an input current $-45\,\mu\mathrm{A} \leq I \leq 45\,\mu\mathrm{A}$ was applied and the output signal was recorded.

Different Frequencies of the Switched Capacitor
In fig. 49 the output signal for swept input currents is shown for different frequencies of the clock and anti-clock signal of the switched capacitor. Moreover linear functions are fitted to the recorded data. It can be seen, that different frequencies of the switched capacitor lead to different output voltages for the same input currents and therefore to different resistances. In table 10 the determined resistances R for the different clock and anti-clock frequencies f_{SC} can be seen in dependence of the theoretically expected values R_{theo} calculated with eq. (3.3). Here the determined resistances also differ significantly from the theoretical expected ones.

Tab. 10: The resistances R determined via the slope of the fit functions in fig. 49 are shown for the frequencies f_{SC} of the switched capacitor in dependence of the theoretically expected values R_{theo}.

f_{SC}(kHz)	R(MΩ)	R_{theo}(MΩ)
500	4.28	0.5
50	8.35	5.0
5	36.22	50.0
2.5	69.70	100.0

The determined resistances differ quite strongly from the theoretical expected ones,

especially for high frequencies. For high frequencies the realized resistances are higher as the expected ones. This could be due to the capacity. For high frequencies it is possible, that the capacity is not charged fully to V_{SC} or $-V_{SC}$. The determined resistances correspond to the behaviour of the produced switched capacitor as shown in fig. 24.

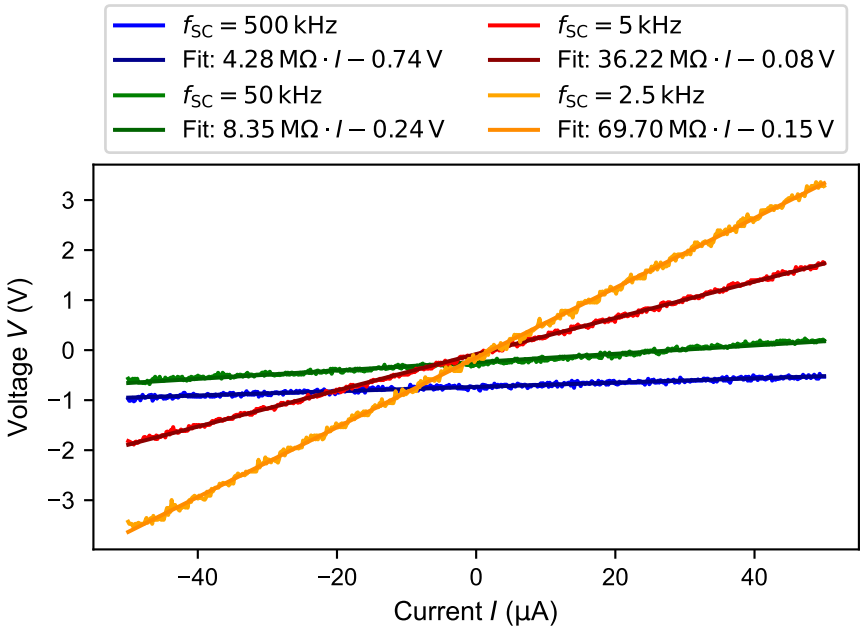
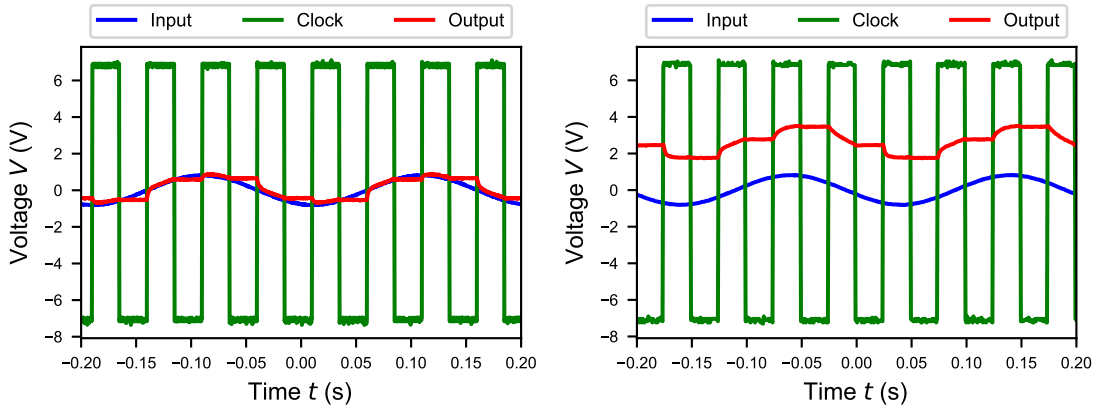


Fig. 49: The output signal of the track and hold circuit with switched capacitor as resistance is shown for a swept input current and different frequencies of the clock and anti-clock signal of the switched capacitor. Additionally linear functions are fitted to the recorded data.

Track and Hold Circuit with and without Input Buffer

In fig. 50 the output, input and square signal at the gate of the transistor (clock signal) are shown for the track and hold circuit and for the track and hold circuit with input buffer.

It is noticeable that the track and hold circuit without buffer is fully functional, as the tracked signal is identical with the input signal and the held signal stays constant. In comparison the track and hold circuit with input buffer shows an offset of approximately 2.5 V and therefore the tracked signal is not equal to the input signal. However the held signal is constant during the holding phases and the circuit is functional in general.

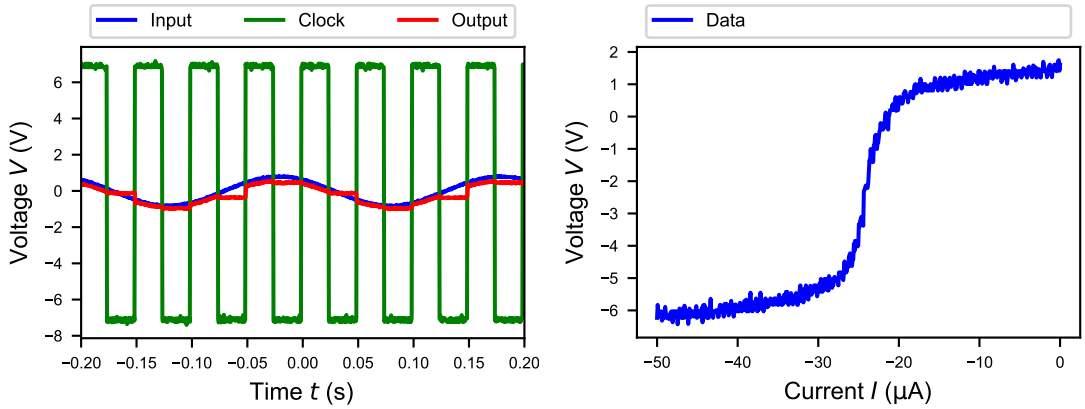


(a) Track and Hold Circuit (b) Track and Hold Circuit with Input Buffer

Fig. 50: The input, output and clock signal at the gate of the transistor are shown. On the left for the track and hold circuit with switched capacitor and on the right with additional input buffer.

Track and Hold Circuit with Output Buffer

In fig. 51 the recorded input, output and clock signal are shown, as well as the output signal for swept input current $-50\,\mu A \leq I \leq 0\,\mu A$ for the track and hold circuit with output buffer.



(a) Track and Hold Circuit with Output Buffer (b) Current sweep

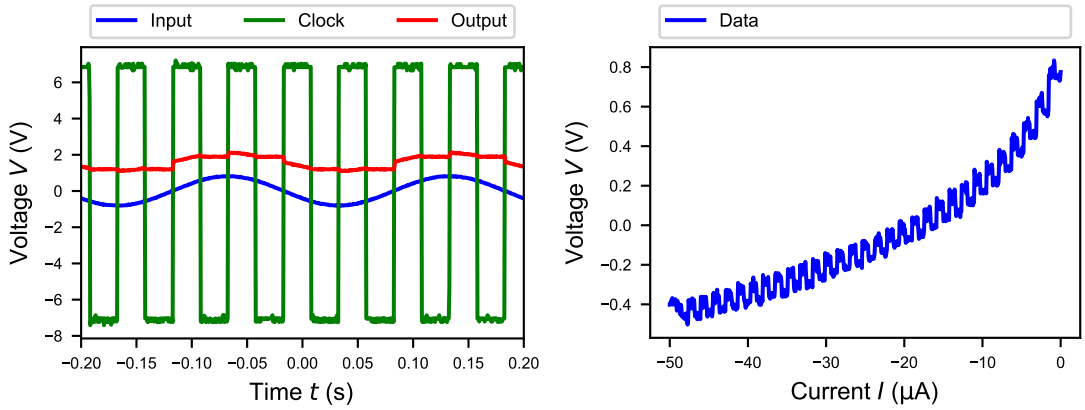
Fig. 51: On the left the input, output and clock signal are shown for the track and hold circuit with switched capacitor and output buffer. On the right the output signal for swept input current is shown for a capacity of 5 pF instead of 10 pF.

The tracked signal corresponds to the input signal and the held signal stays constant during the holding phase. In comparison to the circuit shown in fig. 50, where the clock signal has a frequency of 10 kHz, the clock frequency with output buffer has a frequency of 500 kHz as this circuit is functional even for higher

frequencies. The characteristic between output voltage and input current for this circuit with a capacity of 10 pF is a linear function. For a capacity of 5 pF, the output voltage gets into rail for small and high currents due to the used output buffer. This can be seen in fig. 51 on the right.

Track and Hold Circuit with Input Buffer and Output Buffer

In fig. 52 the recorded input, output and clock signal are shown, as well as the output signal for swept input current $-50\,\mu A \leq I \leq 0\,\mu A$ for the track and hold circuit with input and output buffer.



(a) Track and Hold Circuit with Input and Output Buffer

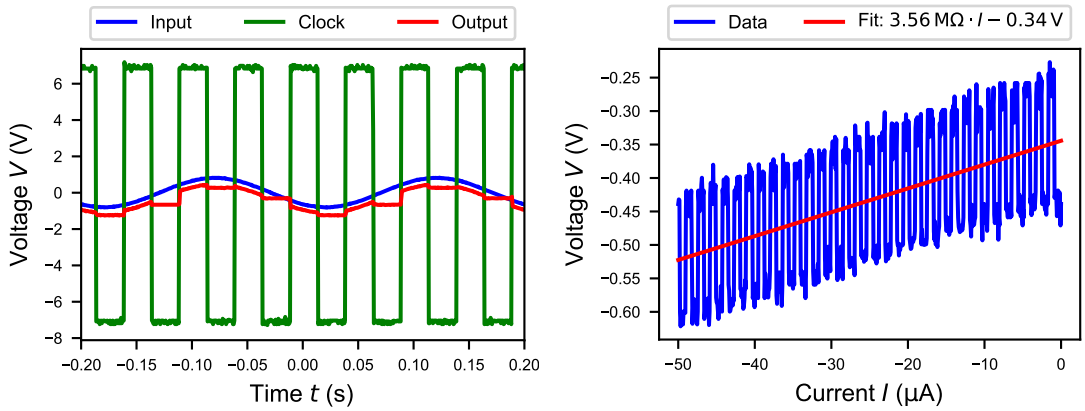
(b) Current sweep

Fig. 52: On the left the input, output and clock signal are shown for the track and hold circuit with switched capacitor and input and output buffer. On the right the output signal for swept input current is shown.

It is noticeable that the output signal has an offset of approximately 1.5 V which could be due to the used buffers. Moreover the characteristic between output voltage and input current is not linear as expected and therefore the circuit is not totally functional. However the held signal stays constant during the holding phase and the tracked signal matches the input signal qualitatively. Like this the circuit is functional in general, but other circuits are favourable to use.

Track and Hold Circuit with Miller Capacity

In fig. 52 the recorded input, output and clock signal are shown, as well as the output signal for swept input current $-50\,\mu A \leq I \leq 0\,\mu A$ for the track and hold circuit with Miller capacity.



(a) Track and Hold Circuit with Miller Capacity (b) Current sweep

Fig. 53: On the left the input, output and clock signal are shown for the track and hold circuit with switched capacitor and Miller capacity. On the right the output signal for swept input current is shown.

The output signal shows a minimal offset in comparison to the input signal which is due to the used buffer in the Miller capacity circuit. However the tracked and held signal are as expected for track and hold circuits and the functionality of this circuit is shown. The output voltage also depends linearly on the input current and the tracking and holding phases can be seen clearly.

4.4.3 Track and Hold Circuits with Transimpedance Amplifier

Another possibility to convert currents into voltages is the use of TIAs. Additionally the input signal can be amplified by choosing the feedback resistance. Therefore TIAs are interesting when small currents want to be measured with track and hold circuits.
The track and hold circuits were produced with TIAs with switched capacitors as variable feedback resistances. To check the functionality of the circuits, a sinus signal with $-400\,\mathrm{mV} \leq V \leq 400\,\mathrm{mV}$ and a frequency of 5 Hz was applied at the input of the track and hold circuit through an external resistor of 10 MΩ. At the gate of the transistor a square signal with $-7\,\mathrm{V} \leq V \leq 7\,\mathrm{V}$ and a frequency of 20 Hz was applied as track and hold signal. Moreover a frequency of 5 kHz was applied at the switched capacitor leading to a theoretical feedback resistance of 50 MΩ. The output signal of the track and hold circuit was measured using an oscilloscope with active probe.

Track and Hold Circuit

In fig. 54 the output signal is shown in red, the input signal in blue and the track and hold signal in green for the track and hold circuit with TIA.

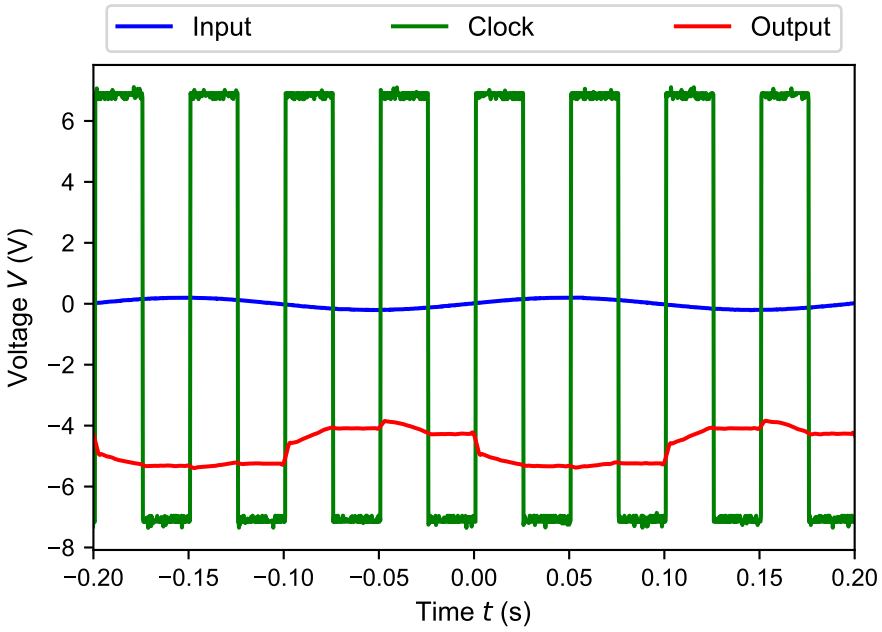


Fig. 54: The input signal of the track and hold circuit with TIA is shown in blue, the output signal in red and the track and hold signal in green.

The output signal is inverted to the input signal and has an offset of approximately $-5\,\mathrm{V}$. This is due to the used TIA. The tracking and holding phases can be seen clearly and the held signal stays constant during the holding phase. The amplitude of the output signal is $1.55\,\mathrm{V}$ leading to a feedback resistance of $38.75\,\mathrm{M\Omega}$ by using eq. (2.11).

Track and Hold Circuit with Output Buffer

As explained in section 2.5.3 output buffers are used to decouple signals and track and hold circuits with output buffers are therefore favourable. In fig. 55 the output, input and track and hold signal of the track and hold circuit with TIA and output buffer is shown.
The tracking and holding phases of the output signal can be seen and the held signal stays constant during the whole holding phase. As expected the output signal is inverted to the input signal and has an offset of approximately $-5\,\mathrm{V}$. The amplitude of the output signal is $2.15\,\mathrm{V}$ leading to a feedback resistance of $53.75\,\mathrm{M\Omega}$. As the theoretical expected feedback resistance is $50\,\mathrm{M\Omega}$ the determined value corresponds very well.

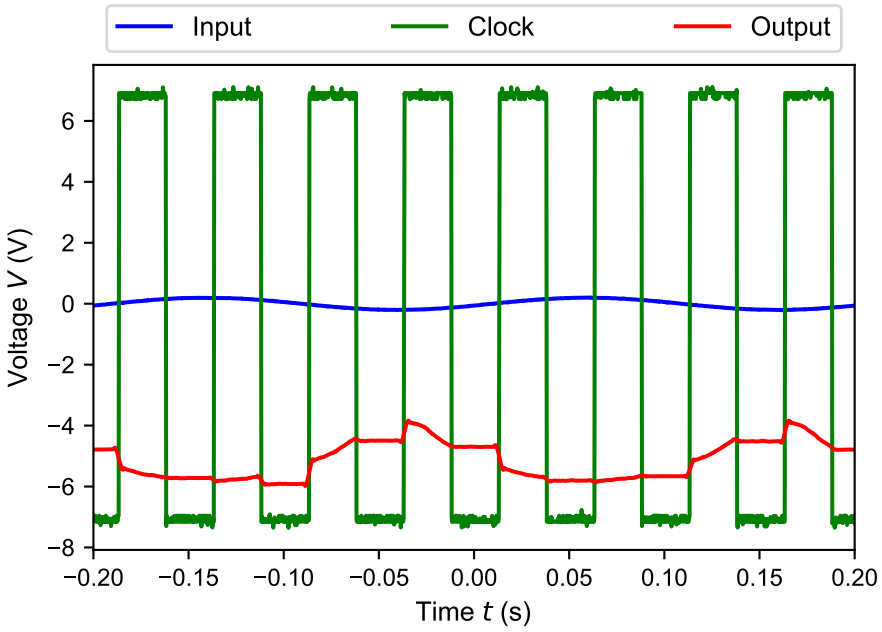


Fig. 55: The input signal of the track and hold circuit with TIA and output buffer is shown in blue, the output signal in red and the track and hold signal in green.

4.5 Track and Hold Circuits with discharged Capacitor

In the different track and hold circuits capacitors are charged by the voltage that wants to be measured. If the capacity is not discharged after the holding phase, the voltage increases further and the tracked signal depends on the current at the capacity. To achieve comparable conditions at the beginning of the different tracking phases, it is necessary to discharge the capacitor after the holding phase. Like this the new tracking phase starts when the capacitor is not charged and the conditions are the same for each tracking phase. This can be realized by adding a transistor, connected to ground for a high gate signal, after the capacity. The circuit diagram is shown in fig. 56.

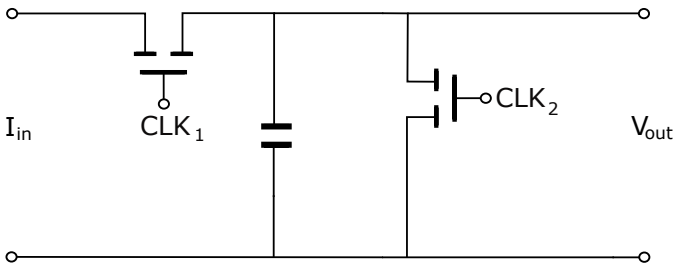


Fig. 56: A track and hold circuit with additional transistor to discharge the capacitor is shown.

To check the functionality of this circuit, a constant input current was applied

as input signal of the track and hold circuit. At the gates of the two transistors square functions with $-10\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ were applied and the output signal of the track and hold circuit was recorded by using the oscilloscope with active probe.
There were three different phases concerning the signals at the gates of the transistors. First the discharge signal was high (CLK_2), then the track and hold signal (CLK_1) was high and then both signals were low. If the track and hold signal is high, the input signal is tracked and if it is low, the tracked signal is held. If the signal at the gate of the transistor discharging the capacity is high, the capacity is discharged. Otherwise the track and hold circuit is not affected by the additional transistor.

In fig. 57 the output signals are shown for different input currents in dependence of the track and hold signal and the discharge signal. The square functions have frequencies of 250 Hz.

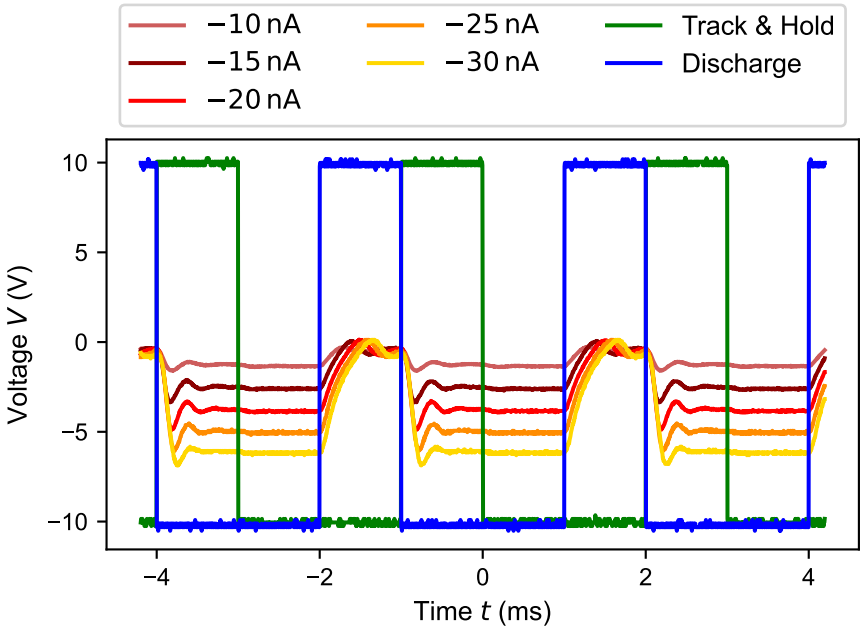
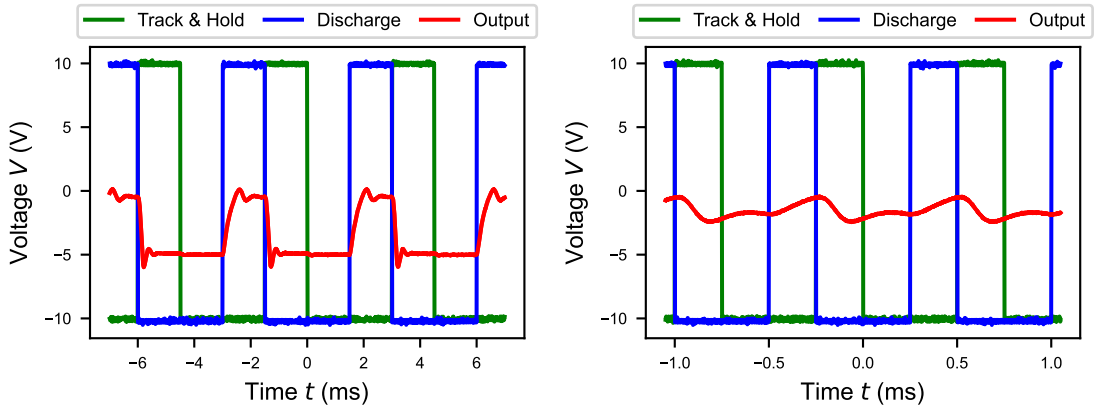


Fig. 57: The output signal of the track and hold circuit with additional transistor to discharge the capacity as shown in fig. 56, is shown for different input currents. In green the track and hold signal and in blue the discharge signal are shown.

The expected behaviour of the output signal for the different phases of the track and hold signal and the discharge signal can be verified. Smaller currents lead to lower output signals in the tracking and holding phase. Additionally, the output signal reaches zero at a faster time during the discharging phase. In comparison, the output signal is higher for higher input currents, but it also takes more time to reach zero during the discharging phase.

In fig. 58 the output signal is shown for different frequencies of the track and hold signal and the discharge signal for an input current of −20 nA.



(a) 222.2 Hz (b) 1.333 kHz

Fig. 58: The output signal of the track and hold circuit with additional transistor to discharge the capacity as shown in fig. 56, is shown in red for different frequencies of the track and hold signal, shown in green, and the discharge signal, shown in blue.

For a low frequency a higher output signal is reached, as the capacity is charged for a longer time. The output signal during the holding phase is constant for both frequencies.

As explained this track and hold circuit is functional in general. Good results are achieved for high input currents and low frequencies of the track and hold signal and the discharge signal. By choosing these parameters correctly, the output signal is high during the tracking phase, constant during the holding phase with nearly no decrease in comparison to the tracked signal and zero after a short time in the discharging phase.

4.6 Track and Hold Circuit with Phototransistors

Phototransistors are useful devices to detect light intensities. When arranged in arrays, spatially resolved measurements of for example laser beams are possible. Therefore it is necessary to create track and hold circuits with phototransistors as shown in fig. 59. In comparison to the track and hold circuits without phototransistor, the phototransistor is added. Additionaly a pull-down resistance needs to be added if no resistance or TIA to convert the current into a voltage, is part of the track and hold circuit.

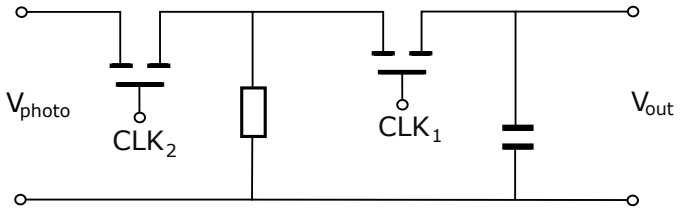
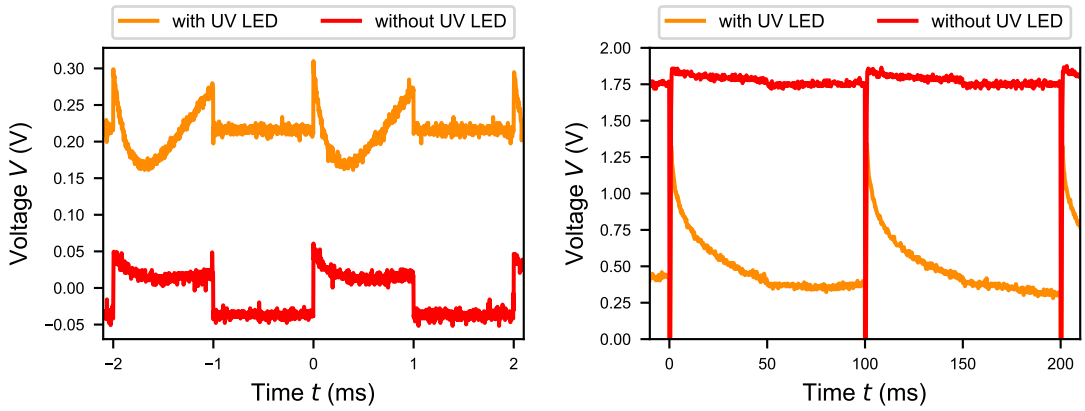


Fig. 59: A track and hold circuit with phototransistor is shown.

To check the functionality of these circuits square functions with voltages $-10\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and frequencies of 500 Hz were applied at the gates of the two transistors. If the potential at the gate of the phototransistor (CLK_2) was low, the potential at the gate of the track and hold transistor (CLK_1) was high and vice versa. For high potentials at the gate of the phototransistor, the phototransistor got fully conductive and was reset when the potential at the gate of the phototransistor was low for the next time. Like that the conditions were the same for each tracking phase. The output signal of the track and hold circuit was recorded using an oscilloscope with active probe. Moreover a LED with ultraviolet light (UV LED) was held over the phototransistor and the output signal of the track and hold circuit was recorded as well. In fig. 60 the recorded output signals with and without UV LED are shown. On the left a track and hold circuit consisting of a transistor and a capacity was used and on the right a track and hold circuit with TIA and square functions with a frequency of 100 Hz were used.



(a) Track and Hold Circuit

(b) Track and Hold Circuit with TIA

Fig. 60: The output signals of the track and hold circuits with phototransistors with applied ultraviolet light are shown in orange and without UV LED in red. On the left a track and hold circuit consisting of a transistor and a capacity was examined and on the right a track and hold circuit with TIA.

For both circuits the tracking and holding phases can be seen. In the holding phases the held signal stays constant and in the tracking phases the signal changes.

For the track and hold circuit consisting of a transistor and a capacity, the output signal without UV LED is approximately 0 V as the phototransistor is not conductive due to the absence of energetic photons. The held signal is lower than the tracked signal and corresponds to the results of section 4.3. By applying ultraviolet light, the phototransistor gets conductive and the output signal increases during the tracking phase. In the holding phase the held signal is constant and a bit lower as the tracked signal.
For the track and hold circuit with TIA the behaviour of the output signal is similar to the one of the track and hold circuit consisting of a transistor and a capacity. As the output signal of a TIA is inverted to the input signal, the output signal of this circuit decreases if the UV LED is used. Additionally an offset of 1.75 V is present due to the TIA, which can be seen especially for the output signal without UV LED.

To examine the track and hold circuits with phototransistors even more, the signals at the gates of the transistors were modified. Instead of symmetrical square functions, asymmetrical ones were used. The high level for each function was two times as long as the low levels. Like that three different phases were created. If the signals at both gates of the transistors were high, the input signal of the track and hold circuit was tracked for a fully conductive phototransistor. Afterwards the track and hold signal was still high to track the signal, but the signal at the phototransistor was low. Like this the phototransistor was reset. In the last phase the track and hold signal was low and the tracked signal in the phase before was held. Like that the phototransistor had no influence on the output signal and the signal at the gate of the phototransistor was chosen high. In fig. 61 the recorded output signal of the track and hold circuit with and without applied ultraviolet light can be seen.
For both cases the general characteristics can be seen. If the signals at the gates of the transistors are both high, the output signal reaches a voltage of 5 V asymptotically. In the next phase, the output signal reaches a voltage of 0 V if no ultraviolet light is applied. In this case the phototransistor is not conductive anymore and like that no signal is present to be detected. If ultraviolet light is applied, the output signal increases after reaching 0 V, as the phototransistor gets conductive due to the energetic photons. In the holding phase, the tracked signal is held for the output signals with and without applied ultraviolet light. As the tracked signal was higher with UV LED, the held signal is also higher in this case.

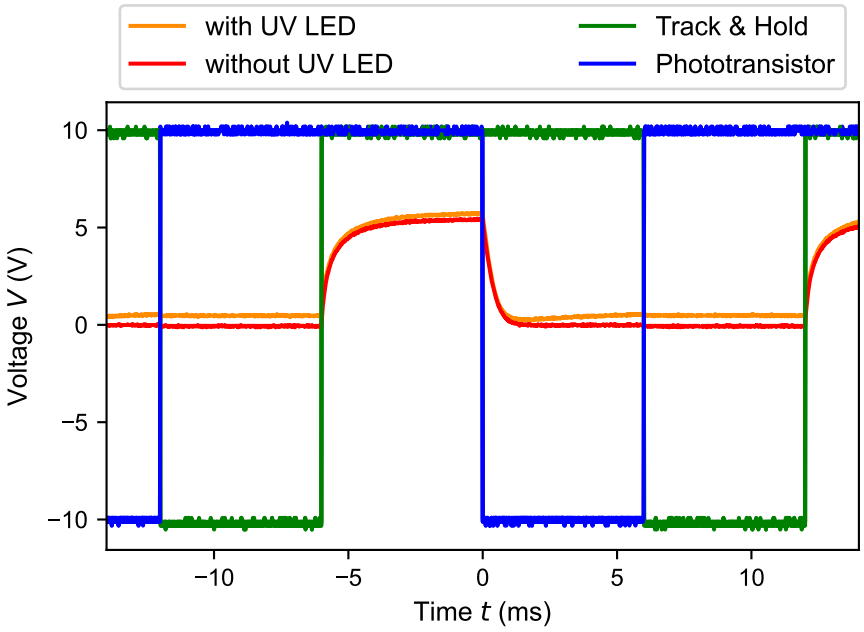
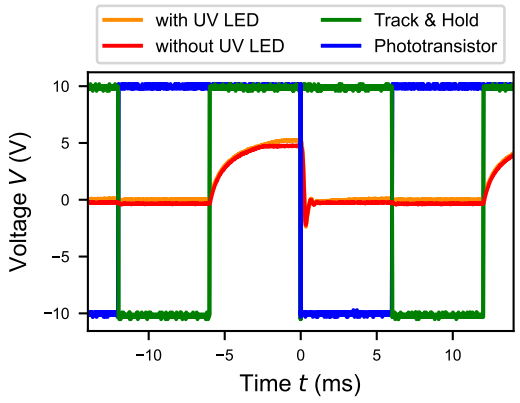
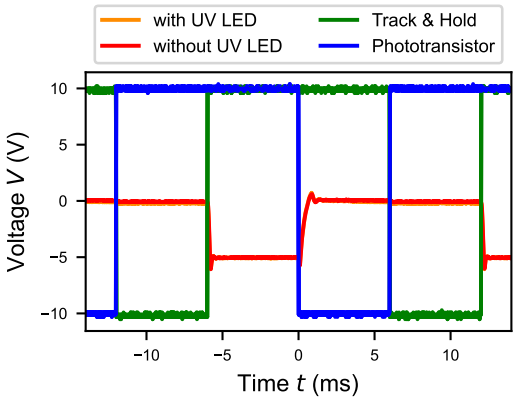


Fig. 61: The output signal of a simple track and hold circuit with phototransistor is shown in red without applied ultraviolet light and in orange for applied ultraviolet light. In green the signal at the gate of the track and hold transistor is shown and in blue the signal at the gate of the phototransistor is shown.

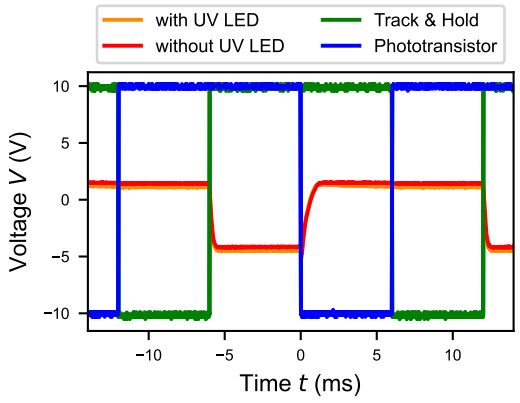
In fig. 62 the output signal for the different phases is shown for different track and hold circuits with phototransistor: with additional output buffer, with TIA and ohmic resistance as feedback resistance, with TIA and switched capacitor as feedback resistance, with TIA and ohmic resistance as feedback resistance and additional output buffer.
For all circuits the output signal with applied ultraviolet light is higher respectively lower if a TIA is used. Therefore all circuits are functional and the output signals are similar to the one shown in fig. 61. For the circuits with TIA the output signal is inverted and has an offset, which is not present when using an output buffer. Moreover the low voltage is reached faster in the phase with low signal at the gate of the phototransistor, if the output buffer is used. However the influence of the applied ultraviolet light is not that high in this case.
For the circuit with TIA and switched capacitor as feedback resistance, it takes longer to reach the low level after the phototransistor is reset. As it is favourable to achieve short reset times, circuits with output buffer and without TIA with a switched capacitor as feedback resistance are the best solution.



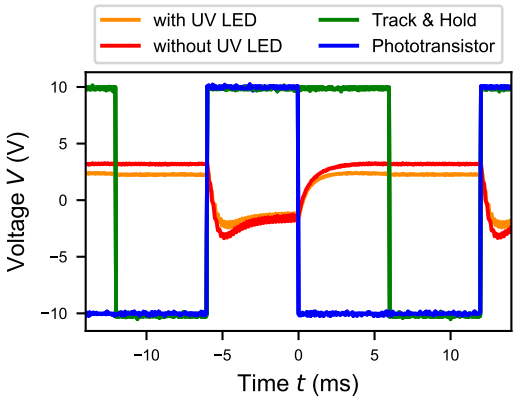
(a) Track and Hold Circuit with Output Buffer



(b) Track and Hold Circuit with TIA and Ohmic Resistance as Feedback Resistance and Output Buffer



(c) Track and Hold Circuit with TIA and Ohmic Resistance as Feedback Resistance



(d) Track and Hold Circuit with TIA and Switched Capacitor as Feedback Resistane

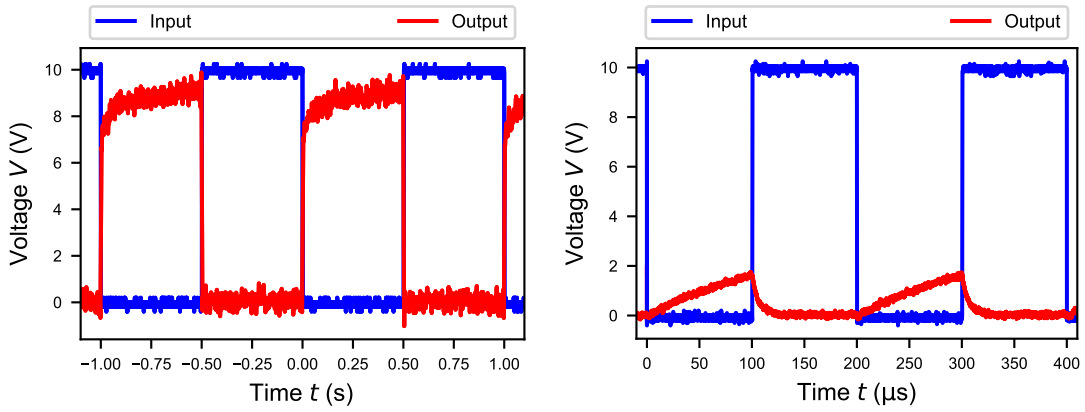
Fig. 62: The output signal of different track and hold circuits with phototransistor are shown in red without applied ultraviolet light and in orange for applied ultraviolet light. In green the signal at the gate of the track and hold transistor is shown and in blue the signal at the gate of the phototransistor is shown.

4.7 Logical Circuits

Logical circuits, like NOT or AND circuits, can be used to realize decoders and multiplexers, which can be used to control for example input and output signals of arrays. In the following the simulated and measured results are presented.
To check the functionality of the logical circuits, square functions with $0\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and different frequencies f were applied at the inputs. The output was recorded by an oscilloscope with active probe.

4.7.1 NOT

The easiest logical circuit is the NOT circuit. Its recorded input and output signal can be seen in fig. 63 for a frequency of 1 Hz on the left and for a frequency of 5 kHz on the right.



(a) $f = 1\,\mathrm{Hz}$ (b) $f = 5\,\mathrm{kHz}$

Fig. 63: The input signal of the NOT circuit is shown in blue and the output signal is shown in red for different frequencies f.

It can be seen, that the circuit is functional, as the output signal is inverted to the input signal. Moreover the output signal needs some time to reach the high or low level due to parasitic capacities in the realized circuit and because of the measuring setup. The high level decreases for higher frequencies of the input signal as the time is too short to charge the capacity. For a frequency of 5 kHz a high level of only 2 V is reached. In this case it is likely that the high level is too low to work as a high level for following circuits or devices.
The high level decreases for increasing frequencies exponentially as seen in fig. 64.

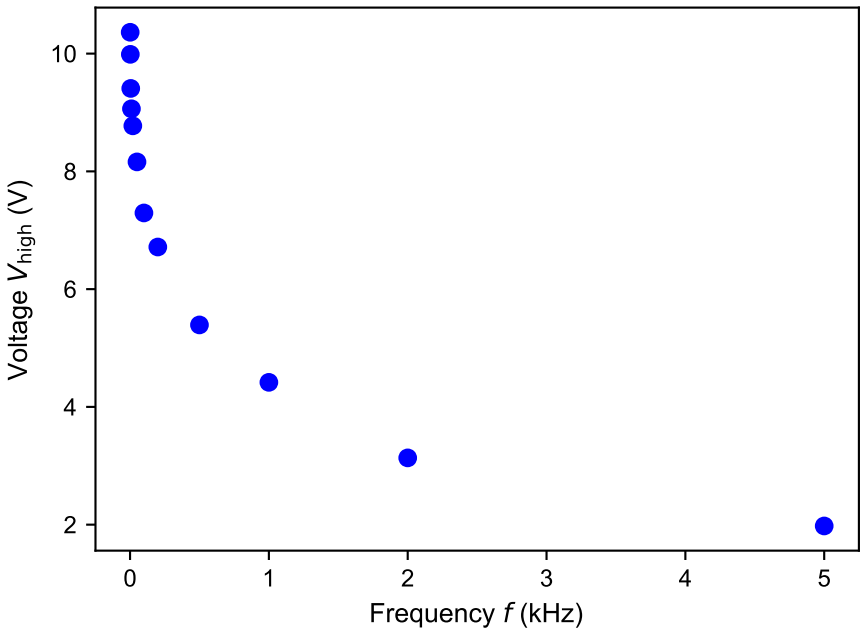
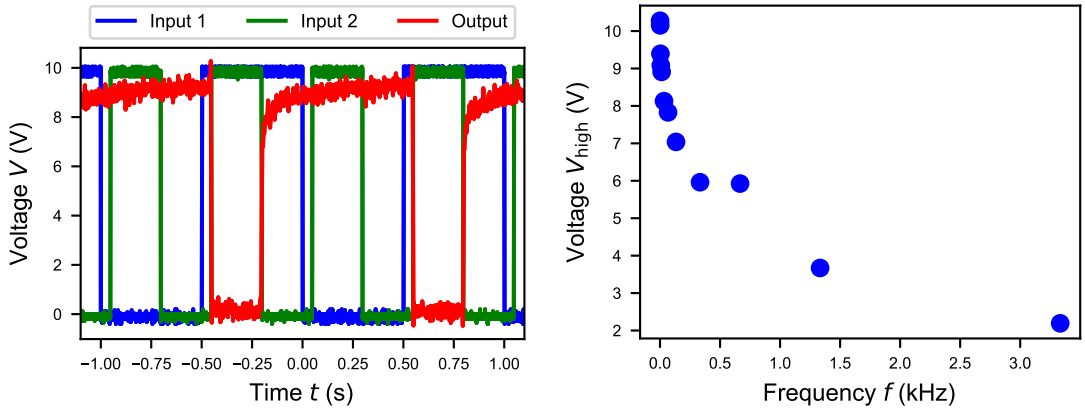


Fig. 64: The high level V_{high} of the output signal of the NOT circuit is shown as a function of the frequency f of the input signal.

4.7.2 NAND

In fig. 65 the recorded output signal of the NAND circuit is shown in dependence of the two input signals on the left. On the right the frequency dependence of the high level is shown.



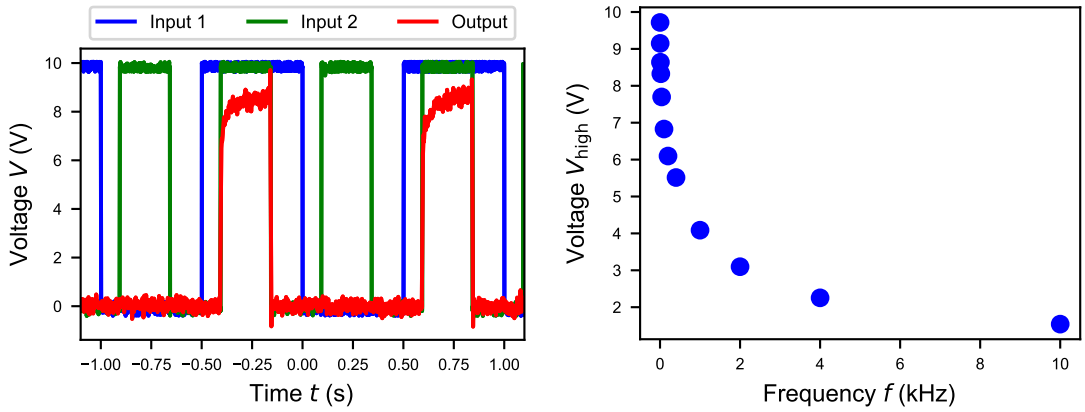
(a) Recorded Signals (b) Frequency Dependence

Fig. 65: On the left the input signals of the NAND circuit are shown in blue and green and the output signal is shown in red. On the right the frequency dependence of the high level V_{high} of the output signal of the NAND circuit is shown.

The output signal is only low if both input signals are high. Otherwise the output signal is high. Therefore the output signal corresponds to the truth table from table 2 and the circuit is functional.
The high level of the output signal decreases for increasing frequencies and the characteristic is similar to the one of the NOT circuit.

4.7.3 AND

In fig. 66 the recorded output signal of the AND circuit is shown in dependence of the two input signals on the left. On the right the frequency dependence of the high level is shown.



(a) Recorded Signals (b) Frequency Dependence

Fig. 66: On the left the input signals of the AND circuit are shown in blue and green and the output signal is shown in red. On the right the frequency dependence of the high level V_{high} of the output signal of the AND circuit is shown.

If both input signals are high, the output signal is high as well. Otherwise the output signal is low, which corresponds to the truth table from table 3. Therefore the circuit is functional.
For increasing frequencies the high level of the output signal decreases analogously to the NOT and the NAND circuit.

4.7.4 Decoder

Decoders can be used to convert n input signals into m output signals.
The produced decoders are not functional due to a layout error. One semiconductor layer in the decoder was bridged and therefore this circuit was not functional. Therefore in the following only the results from the simulation can be discussed. However as decoders are built of NOT and AND circuits and these circuits are functional as explained in section 4.7.1 and section 4.7.3, the decoders should be functional for new substrates without layout error.

Decoder 1:2
In the simulation the enable signal was set high and a square signal with $0\,\mathrm{V} \leq V \leq 9.8\,\mathrm{V}$ was applied as input signal. The high level of the input signal is 9.8 V for better presentation. The output signals in dependence of the enable and the input signal are shown in fig. 67.

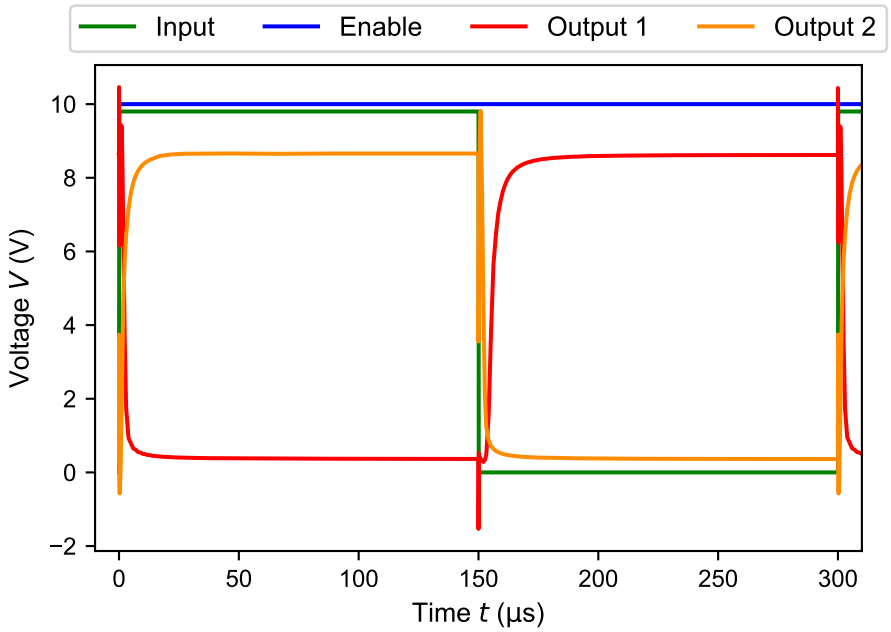


Fig. 67: The signals at the outputs 1 and 2 of the 1:2 decoder are shown in dependence of the input signal and the enable signal.

The output signal one is high if the input signal is low and the output signal two is high if the input signal is high. Like this the output signals correspond to the truth table shown in table 4 and the circuit is functional.

Decoder 2:4
For the 2:4 decoder two different input signals were necessary. A square function with $0\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and frequency f was applied at the input A and a square function with $0.2\,\mathrm{V} \leq V \leq 9.8\,\mathrm{V}$ and frequency $2f$ was applied at the input B. The signals at the outputs 1-4 are shown in fig. 68 in dependence of the input signals.

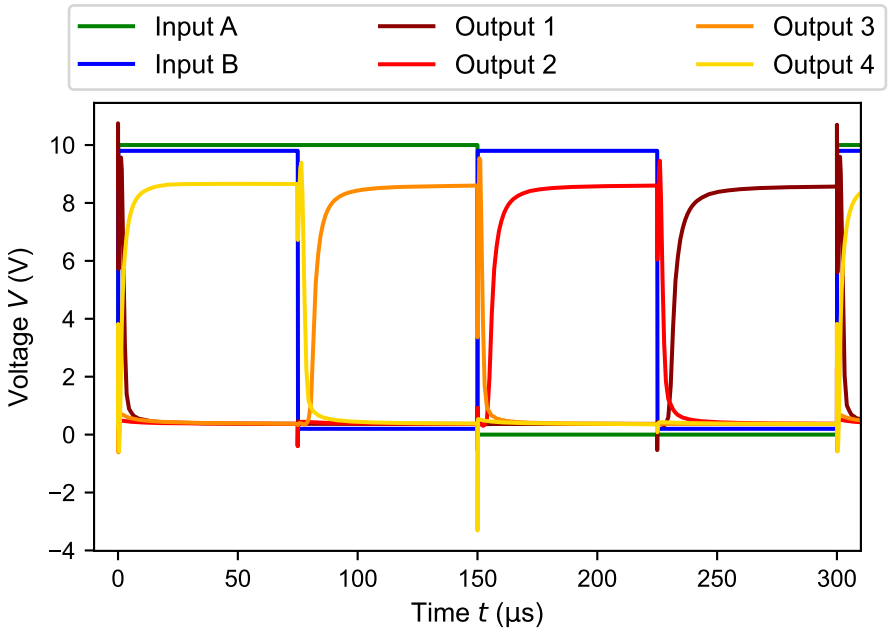


Fig. 68: The signals at the four outputs of the 2:4 decoder are shown in dependence of the two input signals.

The output signal one is high if both input signals are low, the output signal two is high if only the input signal B is high, the output signal three is high if only the input signal A is high and the output signal four is high if both input signals are high. Therefore the functionality of this decoder is shown, as the output signals correspond to the truth table shown in table 5.

Decoder 3:8

To achieve better visibility of the different input signals in the simulation, the high and low levels of the three input signals all have different values. At the input A a square function with $0\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and a frequency f was applied. At the input B a square function with $0.2\,\mathrm{V} \leq V \leq 9.8\,\mathrm{V}$ and a frequency $2f$ was applied and at the input C a square function with $0.4\,\mathrm{V} \leq V \leq 9.6\,\mathrm{V}$ and a frequency $4f$ was applied. The signals at the output 1-8 are shown in fig. 69 in dependence of the input signals.

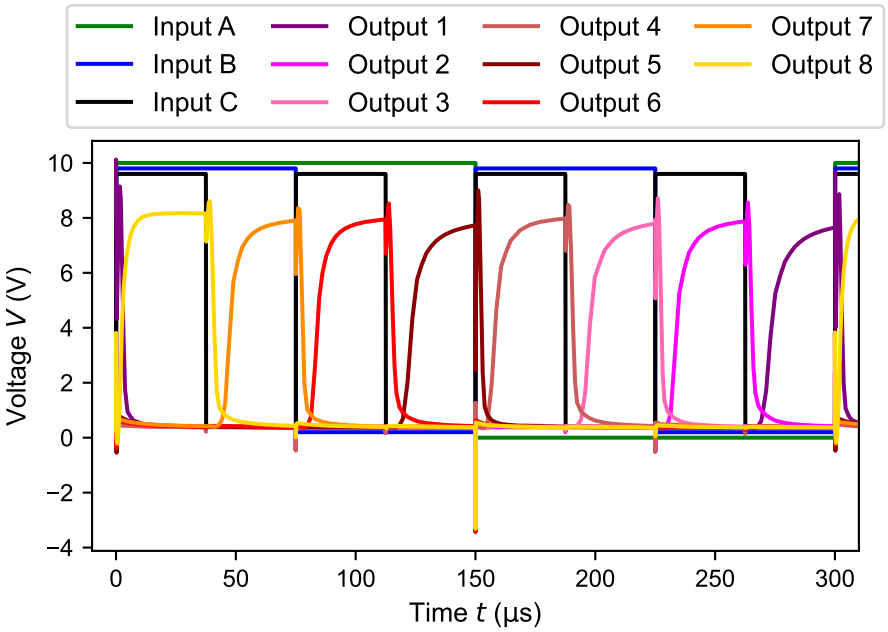


Fig. 69: The signals at the eight outputs of the 3:8 decoder are shown in dependence of the three input signals.

The output signals correspond to the truth table shown in table 6 and therefore this decoder is also functional.

4.7.5 Multiplexer

As multiplexers consist of decoders and additional transistors working as switches, the produced multiplexers were also not functional. However they should as well be functional for a new substrate with fixed layout error.

The 2:1 multiplexer was simulated and the output signal is shown in fig. 70 in dependence of the control signals. The enable signal (Control E) was set high and at the input A of the decoder (Control A) a square function with $0\,\mathrm{V} \leq V \leq 9.8\,\mathrm{V}$ was applied for better visibility in the simulation. At the input one of the multiplexer a potential of 7 V was applied and at the input two of the multiplexer a potential of 1 V was applied.

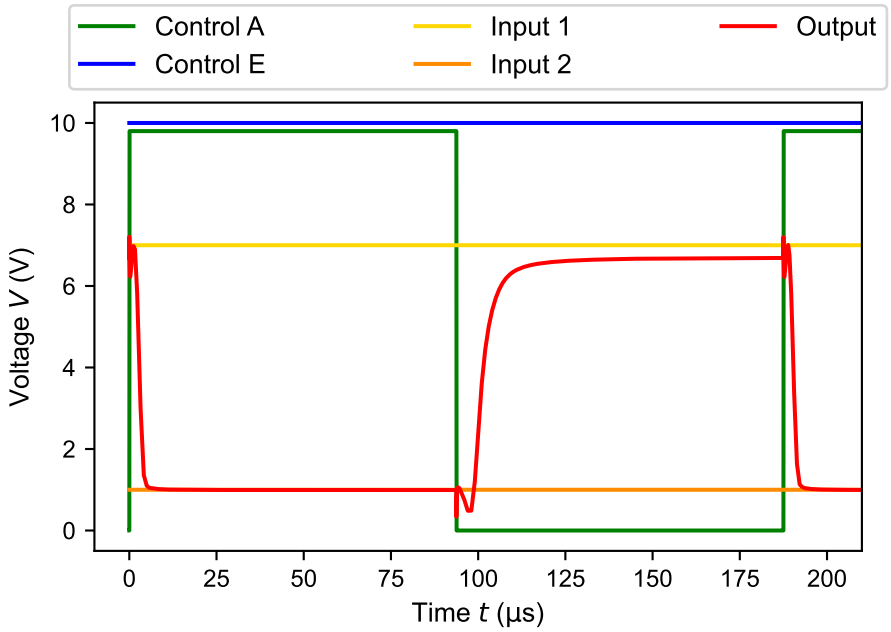


Fig. 70: The output signal of the multiplexer is shown in dependence of the two control signals and the two input signals.

The output signal of the multiplexer shows the expected behaviour. For a high level at the control A signal, the output signal corresponds to the input 2 signal of the multiplexer. For a low level at the control A signal, the output signal corresponds to the input 1 signal of the multiplexer. In this case a slight difference between the voltage levels of the input 1 signal and the output signal is present. This can be explained by the voltage drop off at the transistor.
As the 2:1 multiplexer works, multiplexers of higher order like the 4:1 multiplexer or the 8:1 multiplexer, should work as well and they can be used to control arrays with track and hold pixels. This is shown in section 4.8.1.

4.8 Arrays

Arrays can be used to perform spatially resolved measurements. Therefore the examined track and hold circuits can be used as array pixels. As the aim of the spatially resolved measurement is the detection of ultraviolet light, phototransistors must be used in the track and hold circuits. Moreover the track and hold circuit with output buffer achieved the best results and therefore the array pixels in the following arrays contain phototransistors and track and hold circuits with output buffers.
The arrays are arranged in an active matrix configuration, as shown in fig. 71 for a 2x2 array. The array pixels are connected to the corresponding rows and columns through a TFT working as a switch. By applying a high potential at the corresponding row and measuring the signal at the corresponding column, the output

signal of the chosen array pixel can be measured. For example by applying a high potential at row one and measuring at column one, the output signal of the array pixel 11 can be determined.

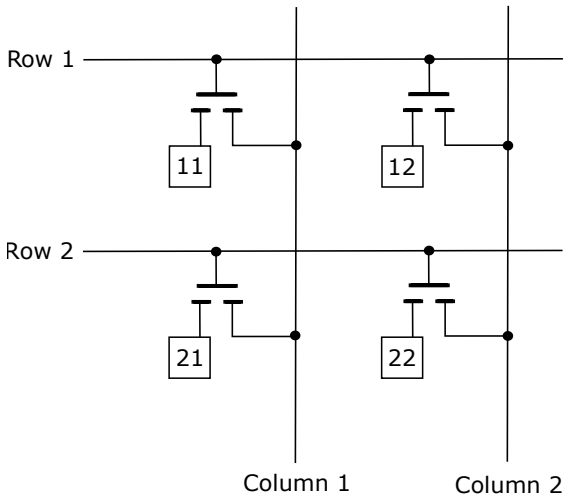


Fig. 71: The circuit design of an active matrix 2x2 array is shown. The squares with the numbers denote the used track and hold circuit as array pixels.

4.8.1 Simulation

In the following the simulated active matrix arrays with and without decoders and multiplexers are discussed.

2x2 Array
For the simulated 2x2 array square signals with $-10\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ with 180° phase shift are applied at the rows. At the gates of the phototransistors different constant potentials are applied, representing different light intensities. For the pixel in row one and column one the applied potential is the lowest, then the potential in row one and column two is the next higher potential, then the potential in row two and column one follows and the potential in row two and column two is the highest. In fig. 72 the signal at the columns are shown in dependence of the signal at the rows.
It can be seen that the signal at the columns is different for the two rows and for the same rows the signal of the two columns is also different. The signals at the columns correspond to the applied potential at the gates of the phototransistors. The signal in row two and column two is the highest and the signal in row one and column one is the lowest. The signal in row one and column two is higher as the one in row one and column one, but lower than the signal in row two and column one. Like this the functionality of the 2x2 array is shown.

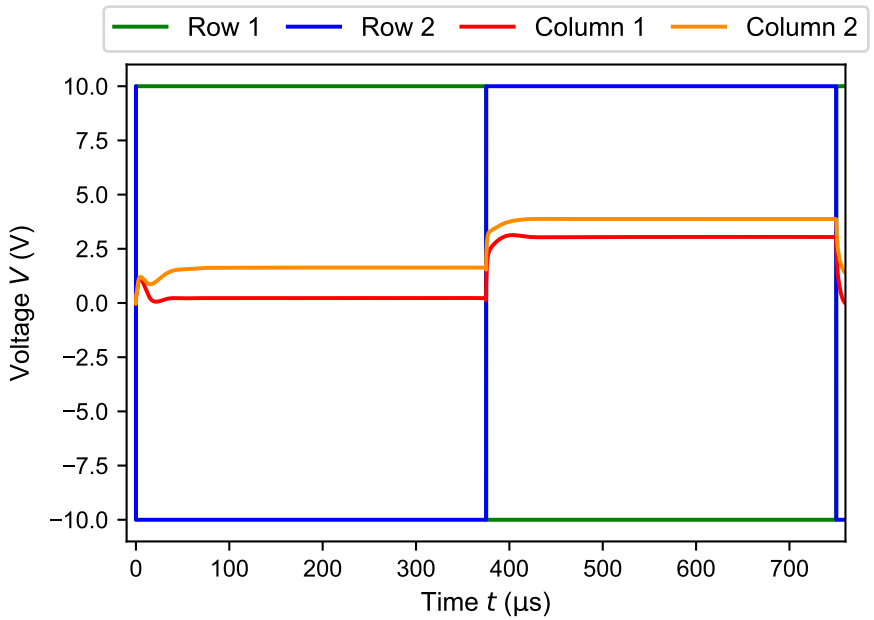


Fig. 72: The signals at the columns of a 2x2 active matrix array are shown in dependence of the signals at the rows of the array.

2x2 Array with Decoder and Multiplexer

It is possible to control arrays with decoders and multiplexers. Like this the array pixel can be chosen by the input signal of the decoder and the control signal of the multiplexer. With the decoder the row is chosen and with the multiplexer the column is chosen. Moreover the output signal of the chosen array pixel is the output signal of the multiplexer. In fig. 73 the circuit for such an array is shown schematically.

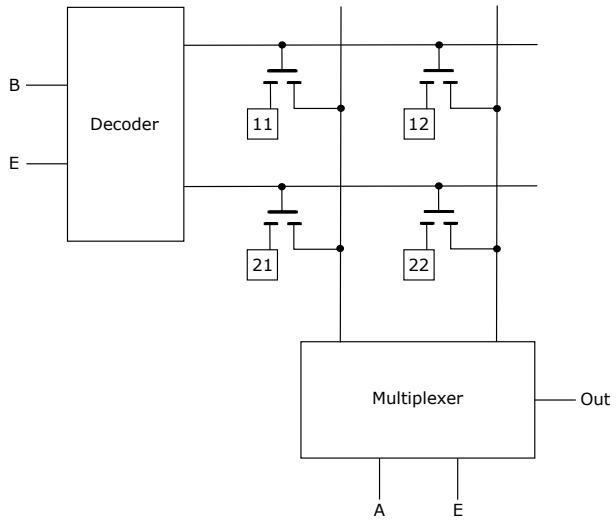


Fig. 73: The circuit design of an active matrix 2x2 array, which is controlled by a decoder and a multiplexer, is shown.

In fig. 74 the output signal of the simulated 2x2 array with decoder and multiplexer is shown in dependence on the input signal of the decoder and the control signal of the multiplexer.

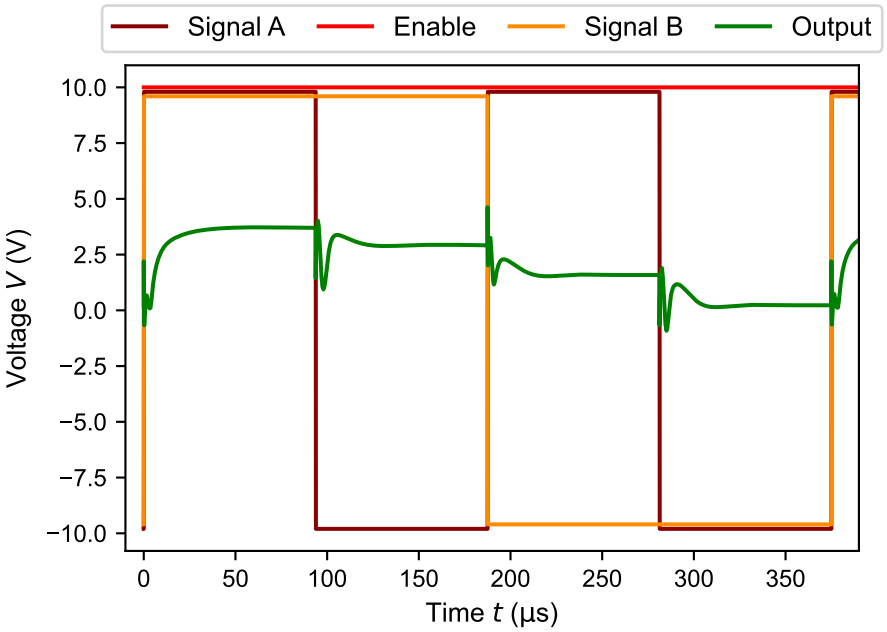


Fig. 74: The output signal of a 2x2 active matrix array, controlled with one decoder and one multiplexer, is shown in dependence of the signals applied at the decoder and the multiplexer.

If the input signal of the decoder (signal B) is low, row one is selected and if it is high, row two is selected. If the control signal of the multiplexer (signal A) is low, column one is selected and if it is high, column two is selected. This can be seen at the output signal as it decreases from the left to the right. First row two and column two is selected, then row two and column one, then row one and column two and lastly row one and column one. The potentials at the gates were not changed in comparison to the 2x2 array without decoder and multiplexer and therefore the output signal corresponds to the applied signals at the gates of the phototransistors.

4x4 Array with Decoder and Multiplexer

Analogously to the 2x2 array with decoder and multiplexer the 4x4 array with decoder and multiplexer can be examined. Therefore at the gates of the phototransistors in the same columns the same potential is applied for a better presentation of the functionality. The potential for column one is the lowest, the potential for column two is higher, the potential for column three is even higher and the potential for column four is the highest. Like that the output signal should be the same for each row. The rows and columns are selected by the decoder and

the multiplexer as for the 2x2 array with decoder and multiplexer. In fig. 75 the output signal is shown in dependence of the selected rows.

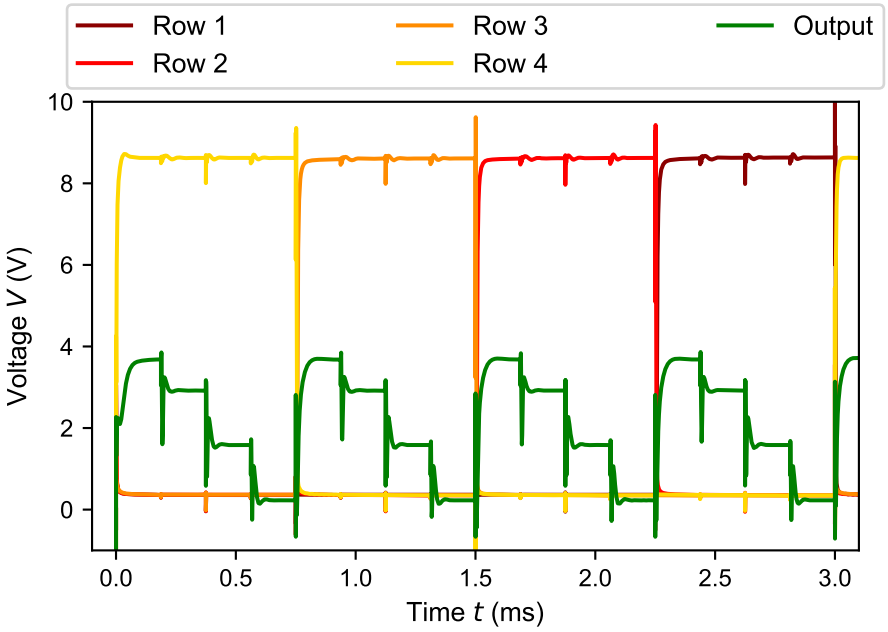


Fig. 75: The output signal of a 4x4 active matrix array, which is controlled with one decoder and one multiplexer, is shown in dependence of the signals at the four rows.

It can be seen that the output signal corresponds to the potential at the gates of the phototransistors for the different pixels in the array. The output signal is the same for each row and decreases for one row as the different columns are selected analogously to the 2x2 array with decoder and multiplexer.

8x8 Array with Decoder and Multiplexer

Analogously to the 4x4 array with decoder and multiplexer, the 8x8 array with decoder and multiplexer was simulated. For each column the same potential was applied at the gate of the phototransistor and the potential was the highest for column eight and the lowest for column one.
The output signal is shown in fig. 76 and corresponds to the expected signal.

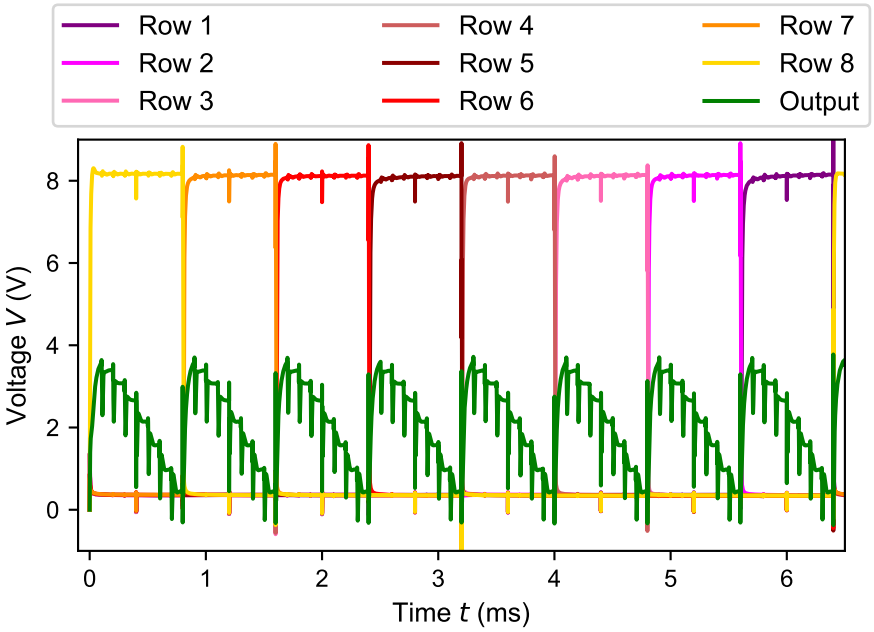


Fig. 76: The output signal of a 8x8 active matrix array, which is controlled with one decoder and one multiplexer, is shown in dependence of the signals at the eight rows.

4.8.2 Measurement Result

The 2x2 array with track and hold circuits with output buffer, phototransistor and pull-down resistance as array pixels was examined. Therefore a potential of 10 V was applied at the drain of the transistor. At the gate of the phototransistor an asymmetrical square function with one pulse of 10 V and two pulses of −10 V was applied. At the gate of the track and hold transistor an asymmetrical square function with two high pulses and one low pulse was applied. All pulses had a time of 24 ms. Like that the phototransistor was reset before each tracking phase. At the rows of the array, clock and anti-clock signals with $-10\,\mathrm{V} \leq V \leq 10\,\mathrm{V}$ and a frequency of 3 Hz were applied. The signal at the columns of the array were recorded by an oscilloscope with active probe. First the array was examined without applied ultraviolet light and then ultraviolet light was applied to the phototransistor in row two and column one of the array.
The voltage differences of the output signal of the array pixels with and without applied ultraviolet light are shown in table 11 and illustrated in fig. 77.

Tab. 11: The voltage differences ΔV between the output signals of the array pixels with and without applied ultraviolet light are shown.

ΔV(mV)	column 1	column2
row 1	50	0
row 2	804	4

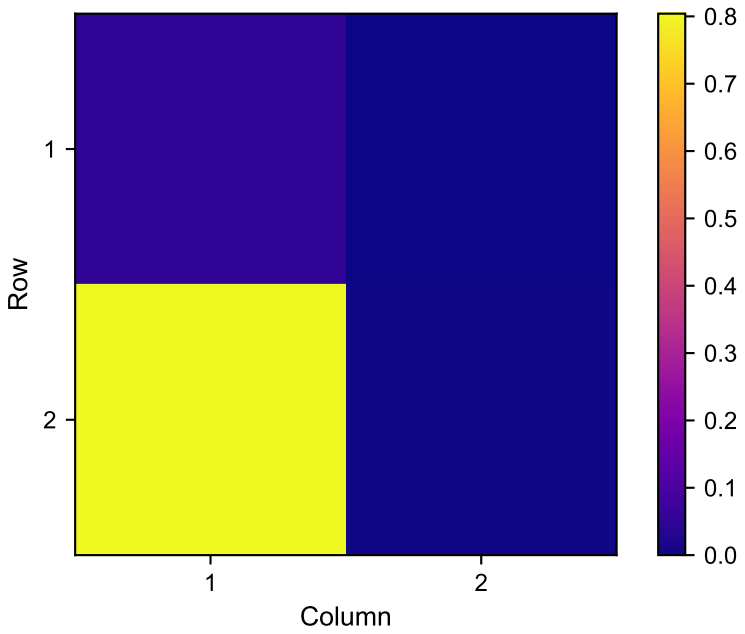


Fig. 77: The voltage difference between the output signals of the array pixels with and without applied ultraviolet light are shown in form of a colormap.

The voltage difference is the biggest for the array pixel in row two and column one, where the ultraviolet light was applied. The voltage difference for the array pixels in column two are nearly zero and for the array pixel in row one and column one, the voltage difference is more than sixteen times smaller than for the one in row two and column one. These results correspond to the position of the used UV LED in row two and column one. As the spatial difference between two array pixels in the same column is not as big as for two array pixels in the same row, the voltage difference for the pixel in row one and column one is higher than for the one in column two and row two.

It can be seen that this array is fully functional and bigger arrays with the same array pixels should work as well. This can be predicted as the arrays should work due to the simulations.

5 Conclusion

5.1 Summary

During this work active matrix arrays for spatially resolved measurements were simulated and examined. They were produced on glass substrates using thin film technology. Track and hold circuits with phototransistors were used as pixels of the arrays.

The circuits were simulated using `AIM Spice` and produced using photolithographic structuring. Therefore lithography masks had to be created.
Ohmic resistances were realized as meander shaped ITO paths and the deviation between the created and theoretically expected resistances was determined to less than 23 % for the resistances between 10 kΩ and 1 MΩ. Moreover resistances were created using switched capacitors. In this case the resistance was adjustable after fabrication, but the bandwidth was limited by half of the frequency of the clock and anti-clock signal.
Capacities were created as overlaps between the drain/source and the top gate layer. The deviation between the actually created capacities and the theoretically expected ones was less than 10 % for the capacities between 1 pF and 10 pF.

IGZO TFTs with a channel length of 10 µm and a channel width of 10 µm respectively 200 µm were created. The characteristics were recorded and it could be shown that the threshold voltage is lower for the TFTs with larger channel width.
Moreover a significant deviation between the TFTs on the different substrates could be noticed. The mobility of the charge carriers varied of a factor 4 and could be explained by different thicknesses of the layers due to an imperfect production.
The characteristics of the realized phototransistors were examined. A significant change in the cut-off region of the transistor was observed if light with energetic photons was applied.

The produced opamp was examined in the open loop configuration, as unity gain amplifier and as TIA. For the open loop configuration a bandwidth of 283 Hz was determined. The unity gain amplifier was functional for frequencies lower than 1 kHz and the TIA was functional for frequencies in the magnitude of 100 Hz.

Different track and hold circuits were examined, i.e. track and hold circuits consisting of a transistor and a capacity, track and hold circuits with input buffer, track and hold circuits with output buffer, track and hold circuits with input buffer and output buffer and track and hold circuits with Miller capacity.
The circuits with Miller capacity and with output buffer were functional for frequencies lower than 1 kHz, whereas the other circuits were only functional for frequencies lower than 500 Hz.
The held signal decreased less, if a higher capacity was used in the track and hold

circuit. Therefore the best results were achieved for a track and hold circuit with output buffer and a capacity of 10 pF.

Input currents were used in combination with track and hold circuits and ohmic resistances, switched capacitors or TIAs to convert the currents into voltages.
By sweeping the input current the ohmic resistances could be determined and compared with the theoretically expected ones. They corresponded quite well for all circuits except the track and hold circuit with input buffer and output buffer and a capacity of 5 pF.
For the track and hold circuits with switched capacitors, an offset of 2.5 V was present for the circuit with input buffer and an offset of 1.5 V for the circuit with input buffer and output buffer.
For the track and hold circuits with TIAs offsets of −5 V were present.

Track and hold circuits with discharged capacitors were used in combination with input currents and without devices to convert the current into a voltage. After each holding phase, the capacitor was discharged to achieve comparable conditions at the start of each tracking phase. Good results were achieved for high input currents and low frequencies of the track and hold signal.

Track and hold circuits with phototransistors were used to detect ultraviolet light. If ultraviolet light was applied, the tracked and held signals were higher as without ultraviolet light.

NOT, NAND and AND circuits were produced and examined concerning their functionality and frequency dependence. All circuits were functional and their high levels decreased with increasing frequency. A bandwidth of 5 kHz was determined.

1:2, 2:4 and 3:8 decoders and multiplexers were simulated and their functionality could be verified. Due to a layout error the realized decoders and multiplexers were not functional and could not be tested.

2x2, 4x4 and 8x8 active matrix arrays were simulated with track and hold circuits with phototransistors and output buffers as array pixels. Their functionality could be verified in the simulation. Additionally the same arrays controlled by one decoder and one multiplexer were simulated and their functionality could be confirmed as well in the simulation.
A 2x2 array was examined physically. Therefore ultraviolet light was applied to the phototransistor in row two and column one and a colormap of the measured data was created. It could be seen, that the signal of the pixel in row two and column one was sixteen times higher as the other signals. Like this the functionality of the produced arrays for spatially resolved measurements was verified.

5.2 Outlook

In future work, the layout of the decoders and multiplexers can be corrected. They can be produced on new substrates and tested concerning their functionality. Additionally the arrays can be controlled with the decoders and multiplexers and their functionality can be examined.

Moreover the realized arrays can be integrated into the setup of the QNOSE project. Therefore a glass cell with the desired array has to be built.
In a first step spatially resolved measurements of the used ultraviolet laser can be performed. Additionally the fluorescence light of the excited nitric oxide molecules can be measured spatially resolved and screenshots of the NO signal can be taken by using arrays of electrodes as measurement arrays.

Another point of future work is the optimization of the used phototransistors. The absorption of ultraviolet light can be increased by changing the thicknesses of the layers of the phototransistor and creating an anti-reflection coating. For optimized phototransistors better results are expected.

6 Appendix

List of Symbols

Symbol	Description
A	amplification
A_0	open loop amplification of an operational amplifier
A_{add}	area of the additional overlap
A_{overlap}	area of the overlap
$\Delta A_{\text{overlap}}$	error of the area of the overlap
C_{diel}	capacity per unity area of the dielectricum
C_{hold}	capacity in the holding phase
$\overline{C_{\text{real}}}$	average value of the actually created capacity
C_{theo}	theoretically expected capacity
ΔC	relative deviation of the capacities
$\Delta C_{\text{produced}}$	error of the produced capacity
d	distance between the two metal layers
ϵ_0	electric field constant
ϵ_r	relative permittivity
f	frequency
f_{SC}	frequency of the switched capacitor
G	gain of an operational amplifier
I	current
I_{D}	drain current of a transistor
I_{in}	input current
l	channel length of a transistor
M	transistor
μ	mobility of the charge carriers
$\overline{\mu}$	average mobility of the charge carriers
N	node
P	phase of an operational amplifier
R	resistance
R_{C}	resistance of the capacity
R_{f}	feedback resistance
R_{real}	actually created resistance
R_{SC}	resistance of the switched capacitor
R_{theo}	theoretically expected resistance
$R_{\square}$	sheet resistance
ΔR	relative deviation of the resistances
ΔR_{SC}	deviation of the resistance of the switched capacitor
t	time
T	Temperature
V	voltage
$V_{\text{C}_{\text{charge}}}$	voltage in the charging process of a capacity

V_{DD}	positive supply voltage
$V_{\mathrm{C_{discharge}}}$	voltage in the discharging process of a capacity
V_{DS}	drain source voltage of a transistor
V_{GS}	gate source voltage of a transistor
V_{high}	voltage of the high level
V_{in}	input voltage
V_{on}	cut-in voltage of a transistor
V_{out}	output voltage
V_{photo}	voltage at the drain of the phototransistor
V_{pp}	voltage amplitude
V_{SC}	voltage between the nodes of a switched capacitor
V_{SS}	negative supply voltage
V_{th}	threshold voltage of a transistor
$\overline{V_{\mathrm{th}}}$	average threshold voltage
V_{-}	inverting input of an operational amplifier
V_{+}	noninverting input of an operational amplifier
ΔV	voltage difference
w	channel width of a transistor

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7 References

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